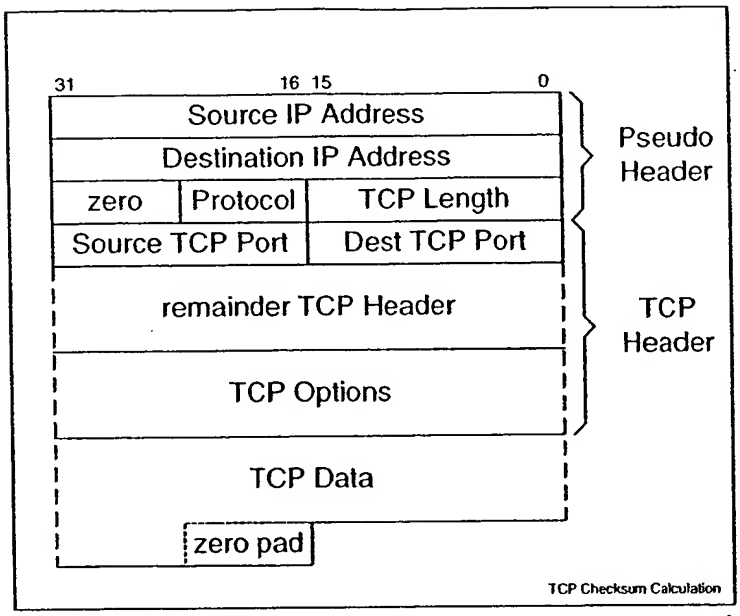


Figure 1A (PRIOR ART)

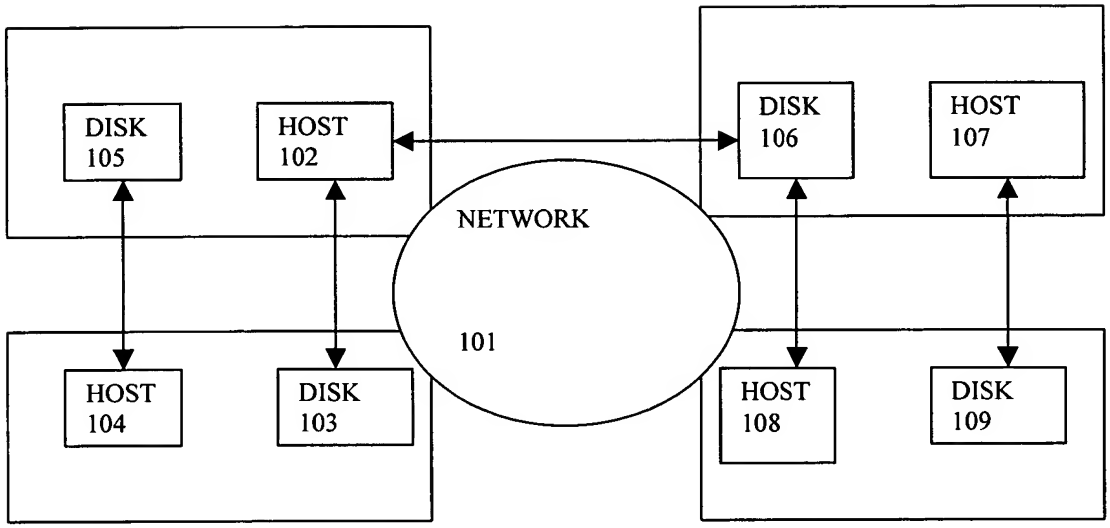

DISK
105
HOST
102
DISK
106
HOST
107
NETWORK
101
HOST
104
DISK
103
HOST
108
DISK
109

FIGURE 2A

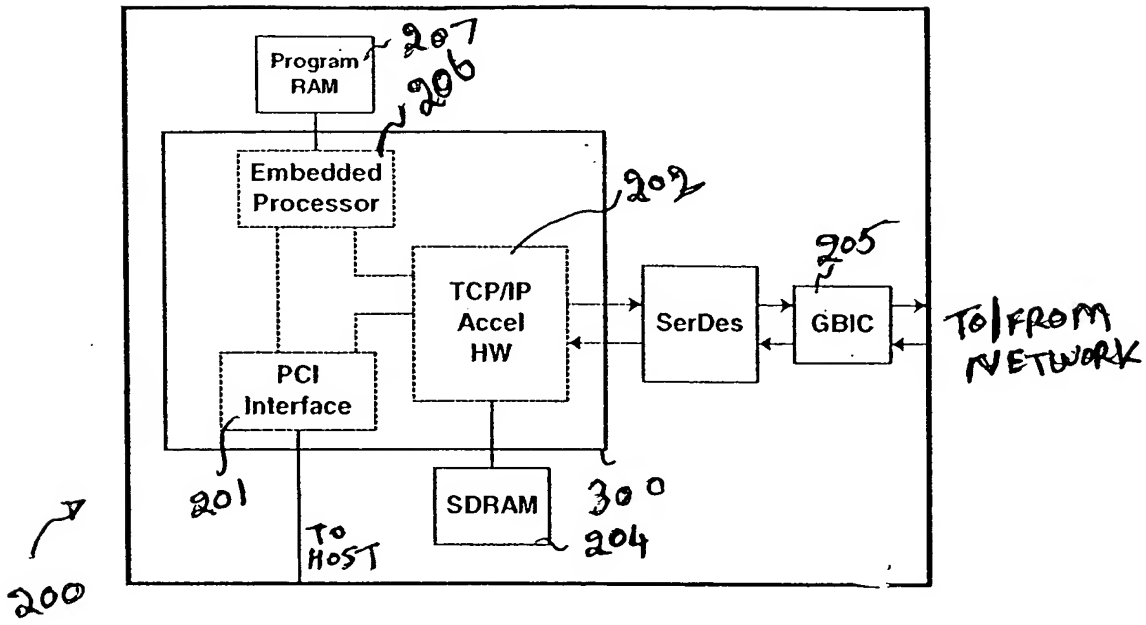


Figure 2B

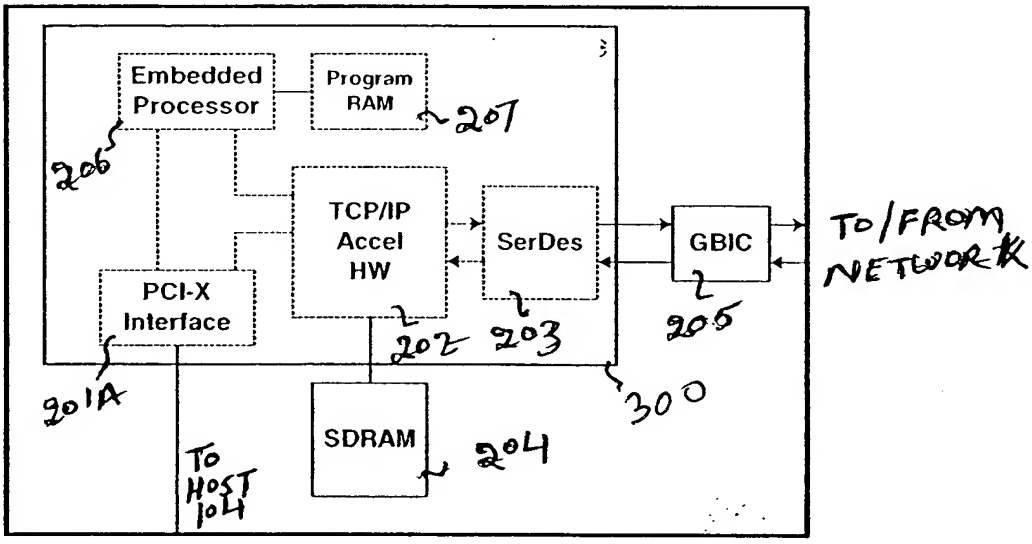


Figure 2C

200A

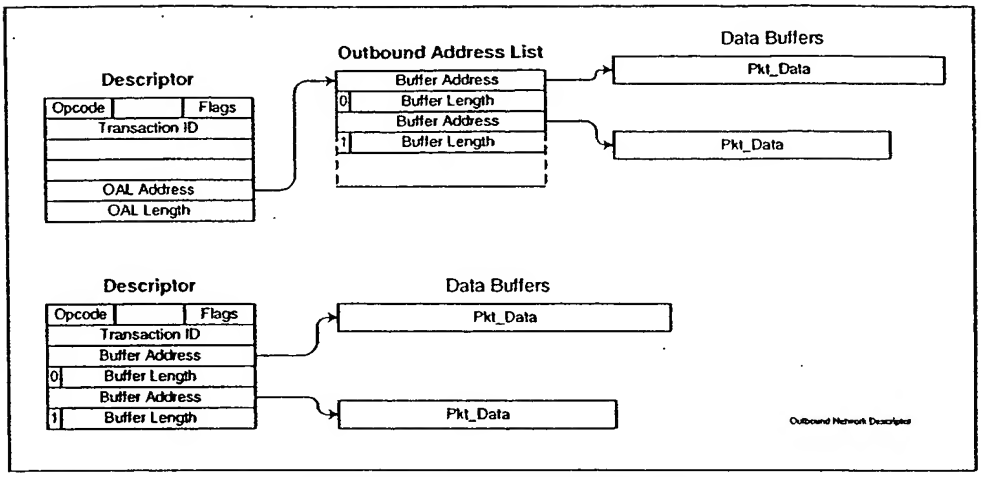


Figure 3A-1 Network IOCB Example

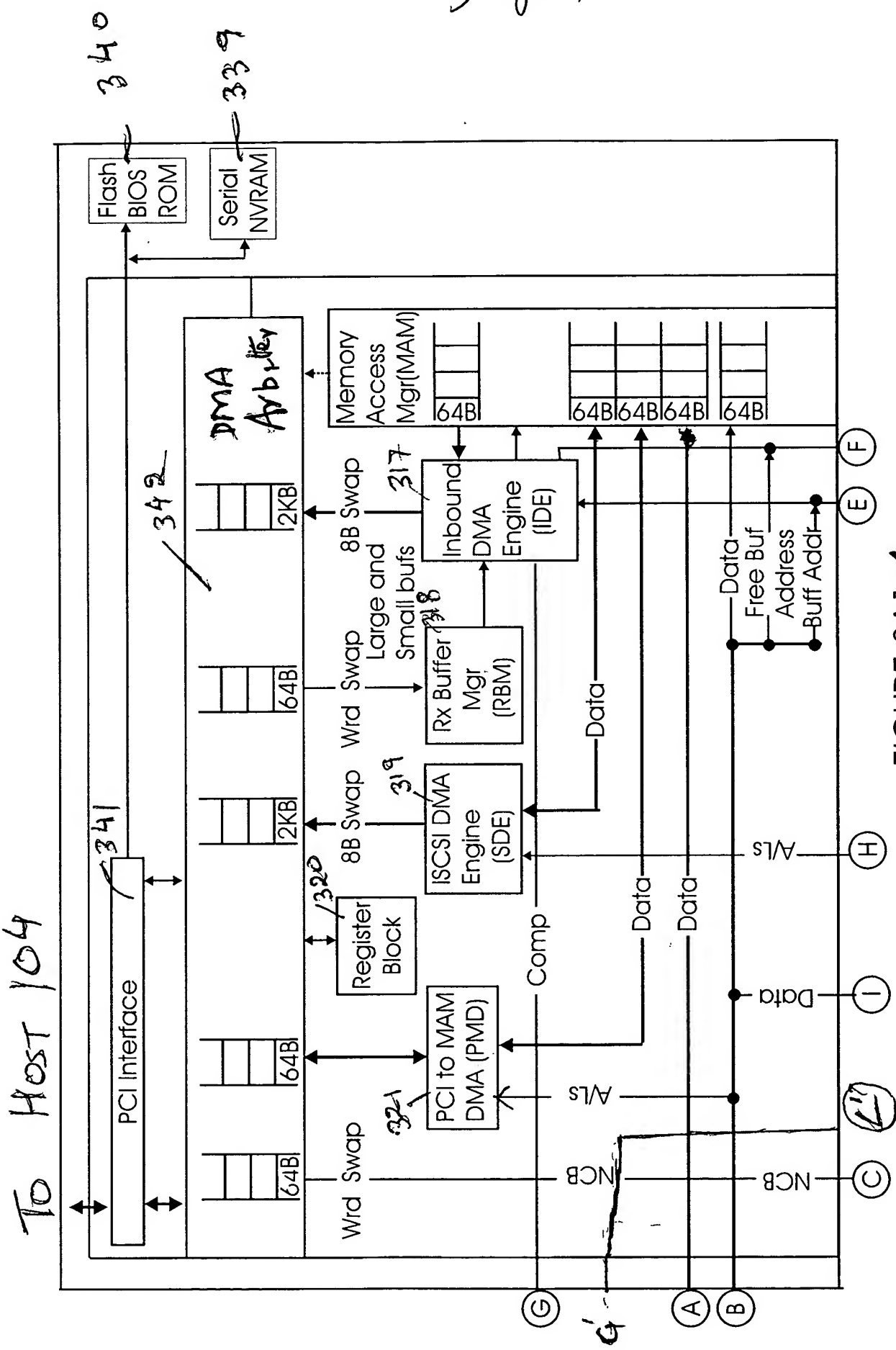

To Host 104
PCI Interface
341
Flash BIOS ROM
340
Serial NVRAM
339
DMA Arbiter
342
Memory Access Mgr(MAM)
64B
64B
64B
64B
64B
2KB
2KB
64B
64B
64B
8B Swap
Large and Small bufs
Wrd Swap
8B Swap
Wrd Swap
317
Inbound DMA Engine (IDE)
318
Rx Buffer Mgr (RBM)
319
ISCSI DMA Engine (SDE)
320
Register Block
321
PCI to MAM DMA (PMD)
Data
Free Buf
Address
Buff Addr
Data
Data
Comp
Data
A/LS
A/LS
Data
NCB
NCB
E
F
H
I
C
G
G'
A
B

FIGURE 3A1-1

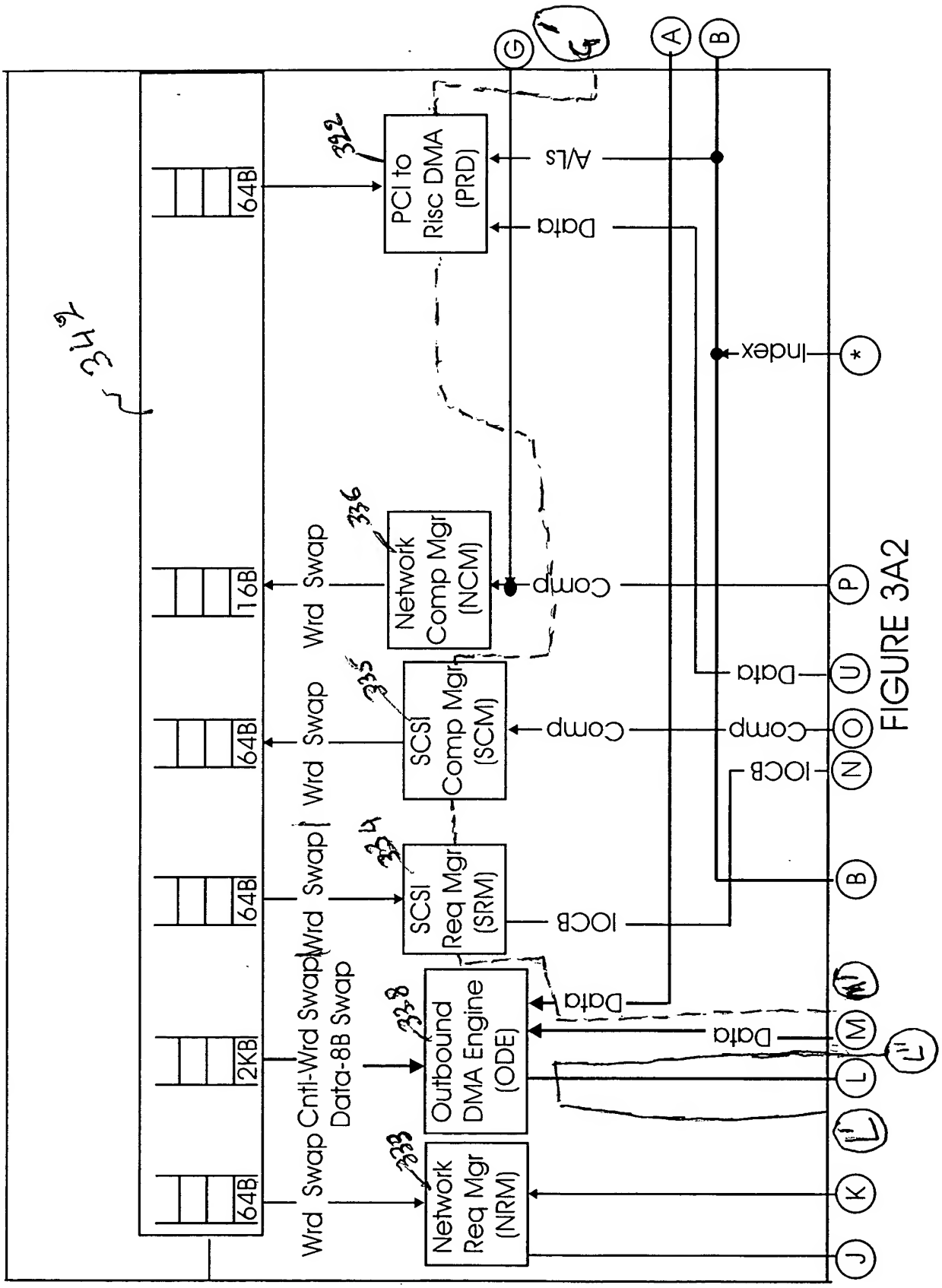

342
64B
64B
64B
64B
2KB
16B
64B
Wrd Swap
Wrd Swap
Wrd Swap
Wrd Swap
Cntl-Wrd Swap
Data-8B Swap
Wrd Swap
PCI to Risc DMA (PRD)
Network Comp Mgr (NCM)
SCSI Comp Mgr (SCM)
SCSI Req Mgr (SRM)
Outbound DMA Engine (ODE)
Network Req Mgr (NRM)
A/Ls
Data
Index
Comp
Data
Comp
IOCB
IOCB
Data
Data
G
A
B
*
P
U
O
N
B
M
L
K
J
L'
L''
M'
332
336
335
334
338
333

FIGURE 3A2

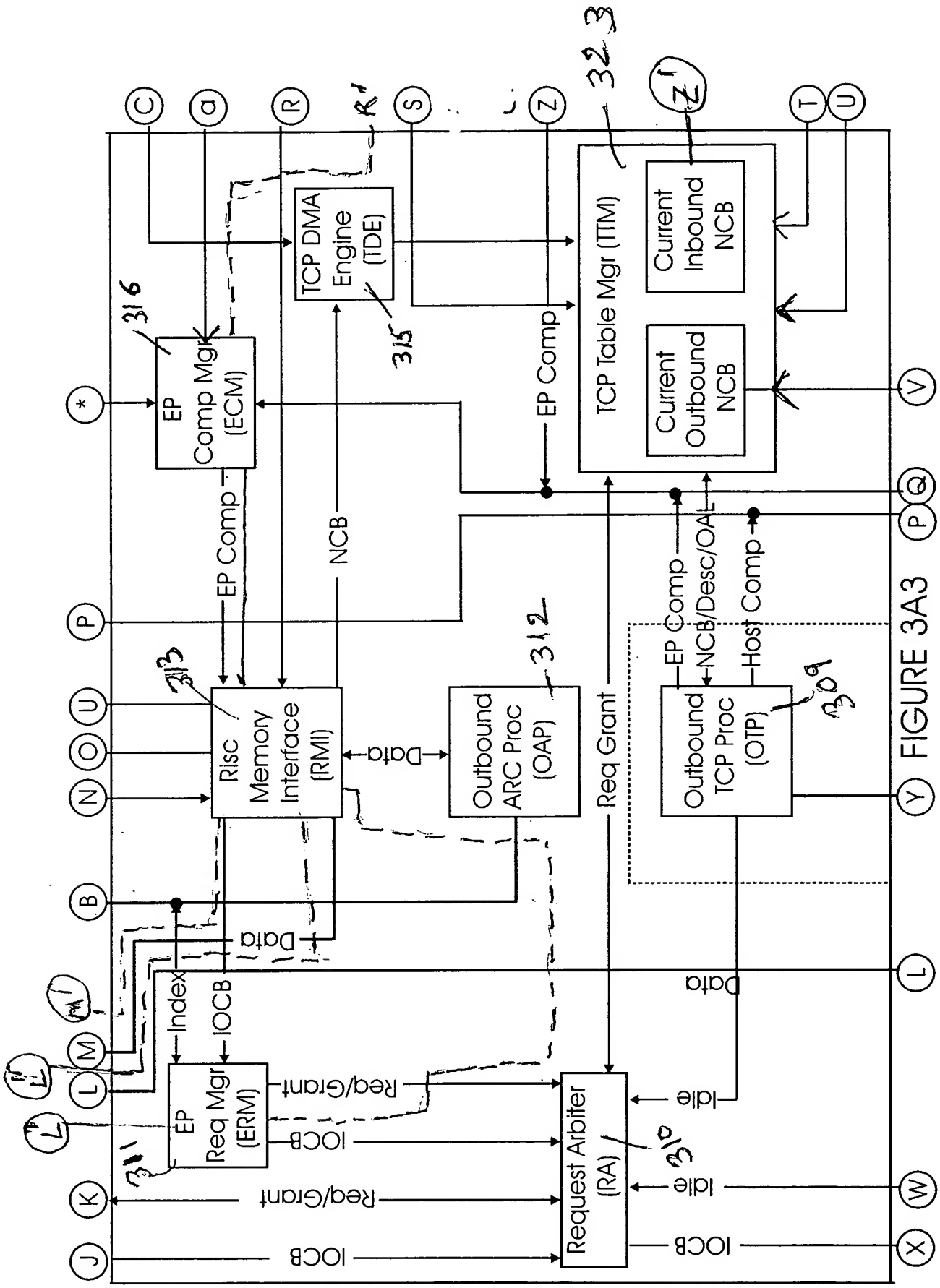

EP Comp Mgr (ECM)
316
TCP DMA Engine (TDE)
315
TCP Table Mgr (TTM)
323
Current Inbound NCB
Current Outbound NCB
EP Comp
NCB
EP Comp
NCB/Desc/OAL
Host Comp
Risc Memory Interface (RMI)
313
Outbound ARC Proc (OAP)
312
Outbound TCP Proc (OTP)
309
Req Grant
Data
Index
IOCB
EP Req Mgr (ERM)
311
Request Arbiter (RA)
310
Idle
IOCB
Req/Grant
C
a
R
R'
S
Z
Z'
T
U
*
V
P
Q
U
O
N
B
M
L
K
J
W
X
Y

FIGURE 3A3

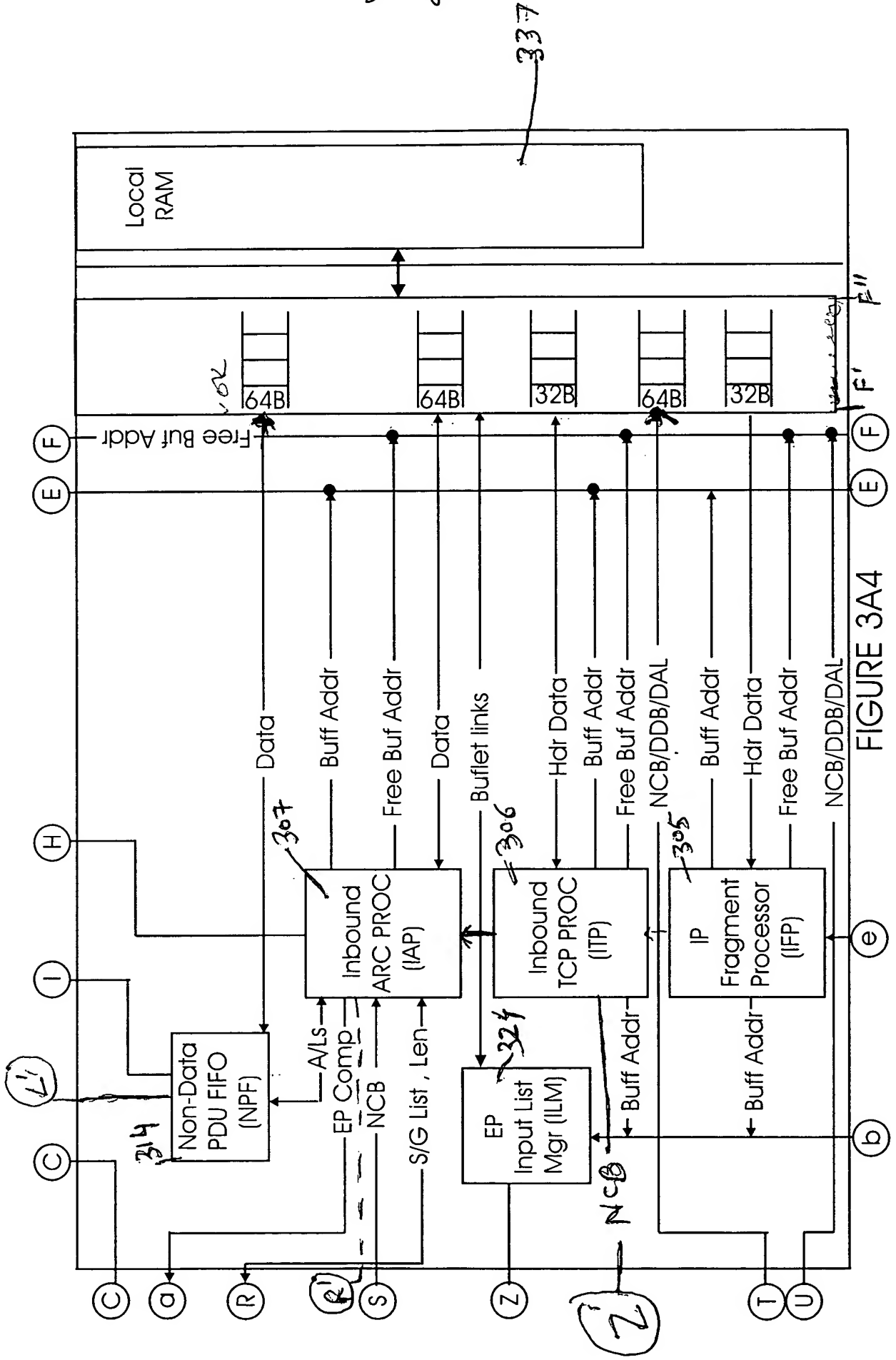

337
Local RAM
64B
64B
32B
64B
32B
Free Buf Addr
Data
Buff Addr
Free Buf Addr
Data
Buflet links
Hdr Data
Buff Addr
Free Buf Addr
NCB/DDB/DAL
Buff Addr
Hdr Data
Free Buf Addr
NCB/DDB/DAL
307
306
305
Inbound ARC PROC (IAP)
Inbound TCP PROC (ITP)
IP Fragment Processor (IFP)
Non-Data PDU FIFO (NPF)
314
A/Ls
EP Comp
NCB
S/G List , Len
EP Input List Mgr (ILM)
324
Buff Addr
Buff Addr
NCB
E
F
H
I
C
a
R
S
Z
T
U
e
b

FIGURE 3A4

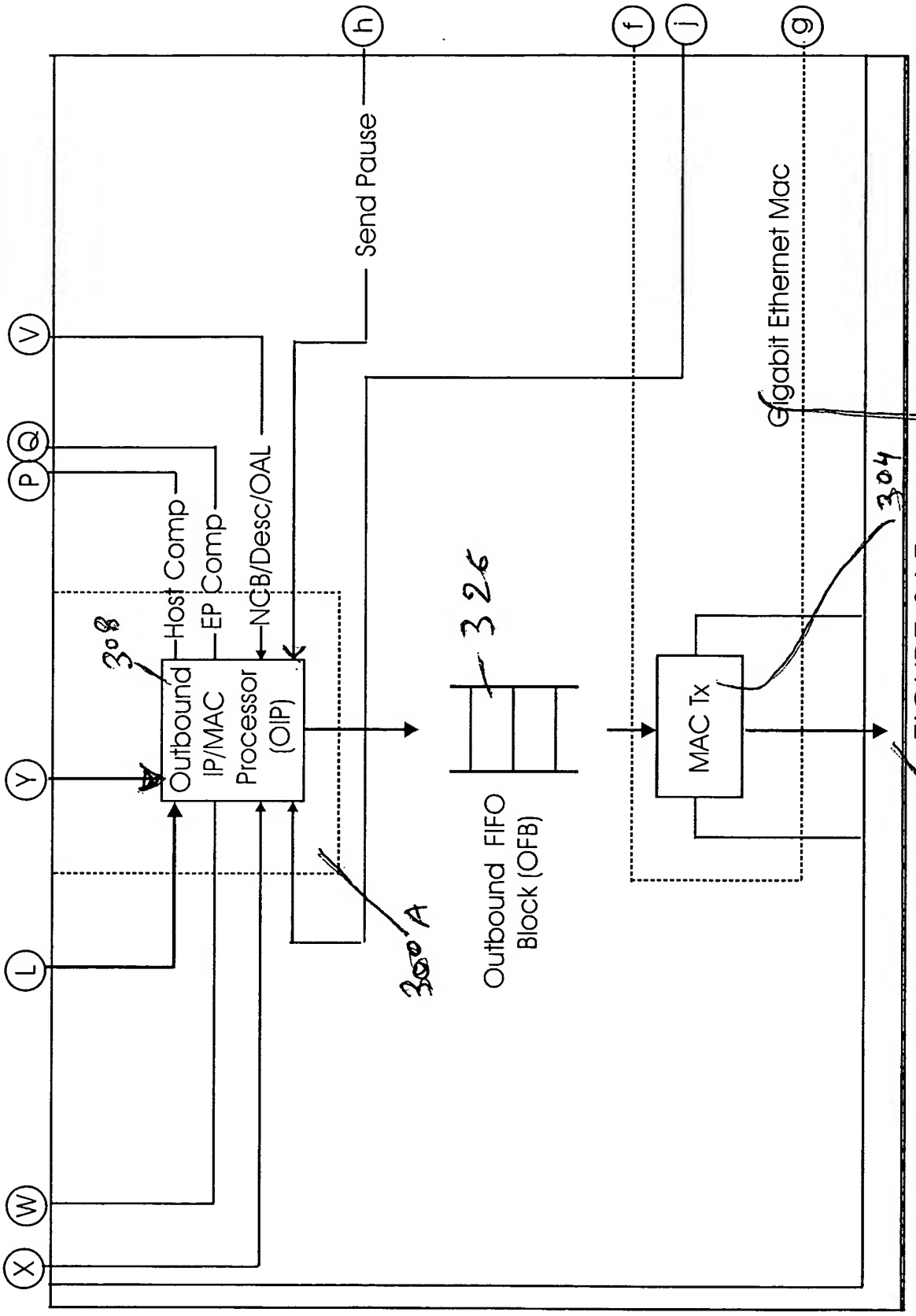

h
f
j
g
Send Pause
Gigabit Ethernet Mac
304 A
V
P
Q
Host Comp
EP Comp
NCB/Desc/OAL
308
Outbound IP/MAC Processor (OIP)
326
304
Y
MAC Tx
L
300 A
Outbound FIFO Block (OFB)
W
X
303 B

FIGURE 3A5

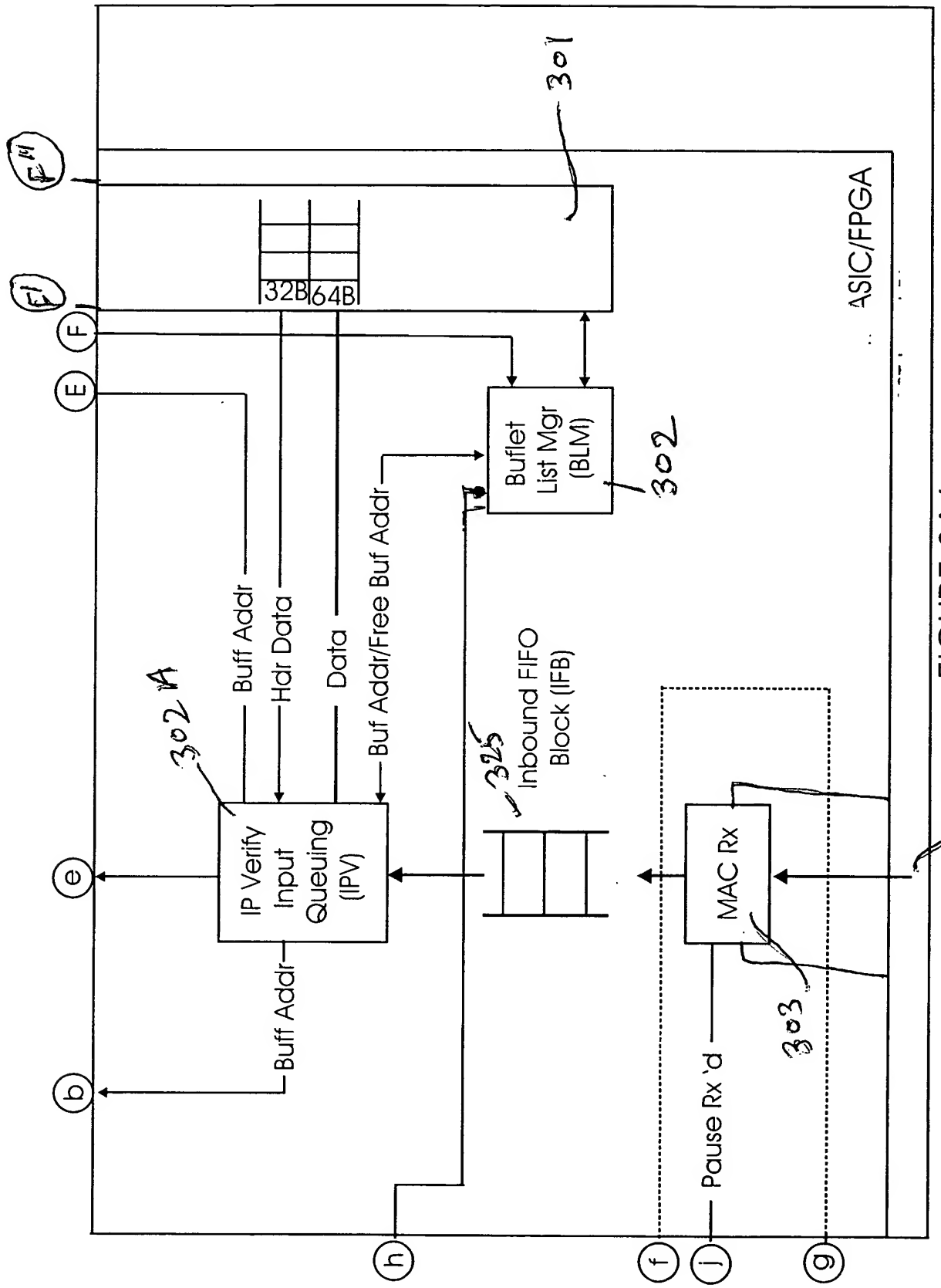
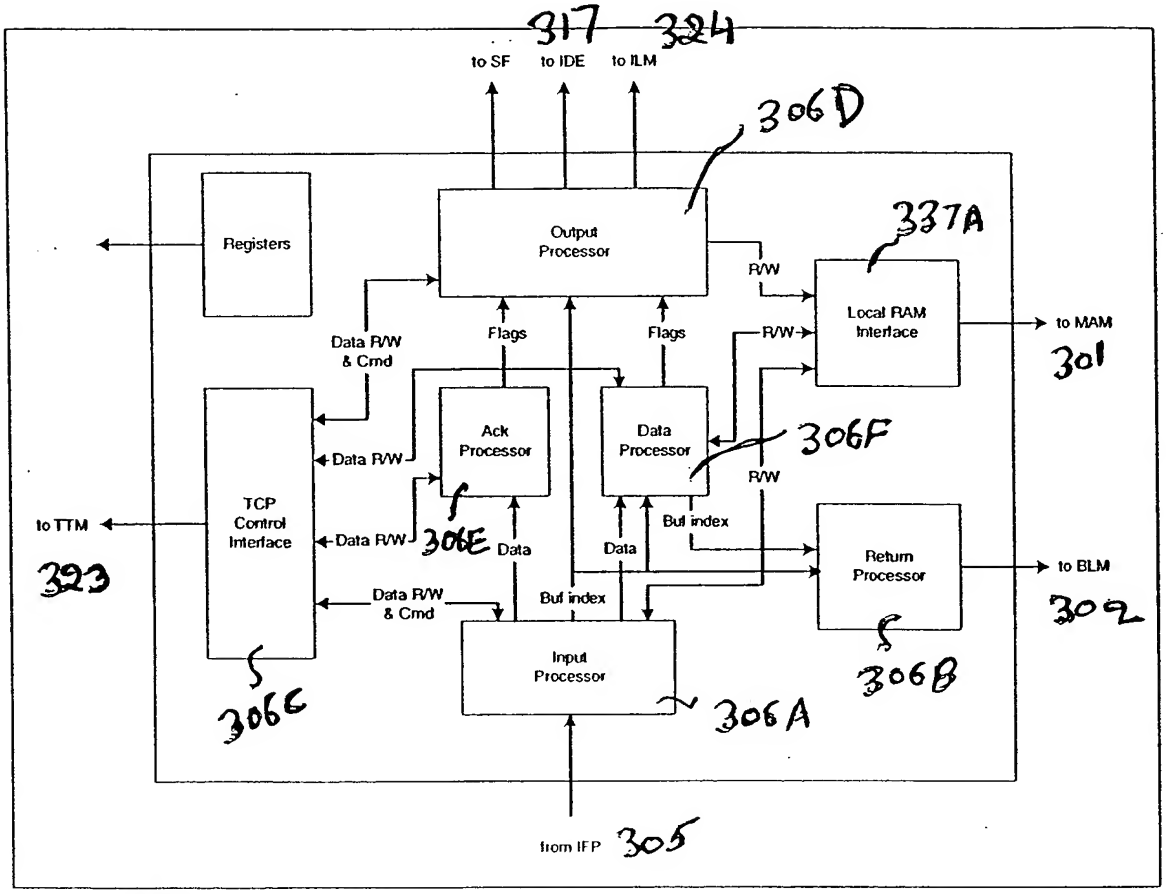

ASIC/FPGA
301
32B
64B
Buflet List Mgr (BLM)
302
Buff Addr
Hdr Data
Data
Buf Addr/Free Buf Addr
302A
IP Verify Input Queuing (IPV)
Buff Addr
325
Inbound FIFO Block (IFB)
MAC Rx
331
303
Pause Rx 'd
E
F
e
b
h
f
j
g

FIGURE 3A6



306

Figure 3B -

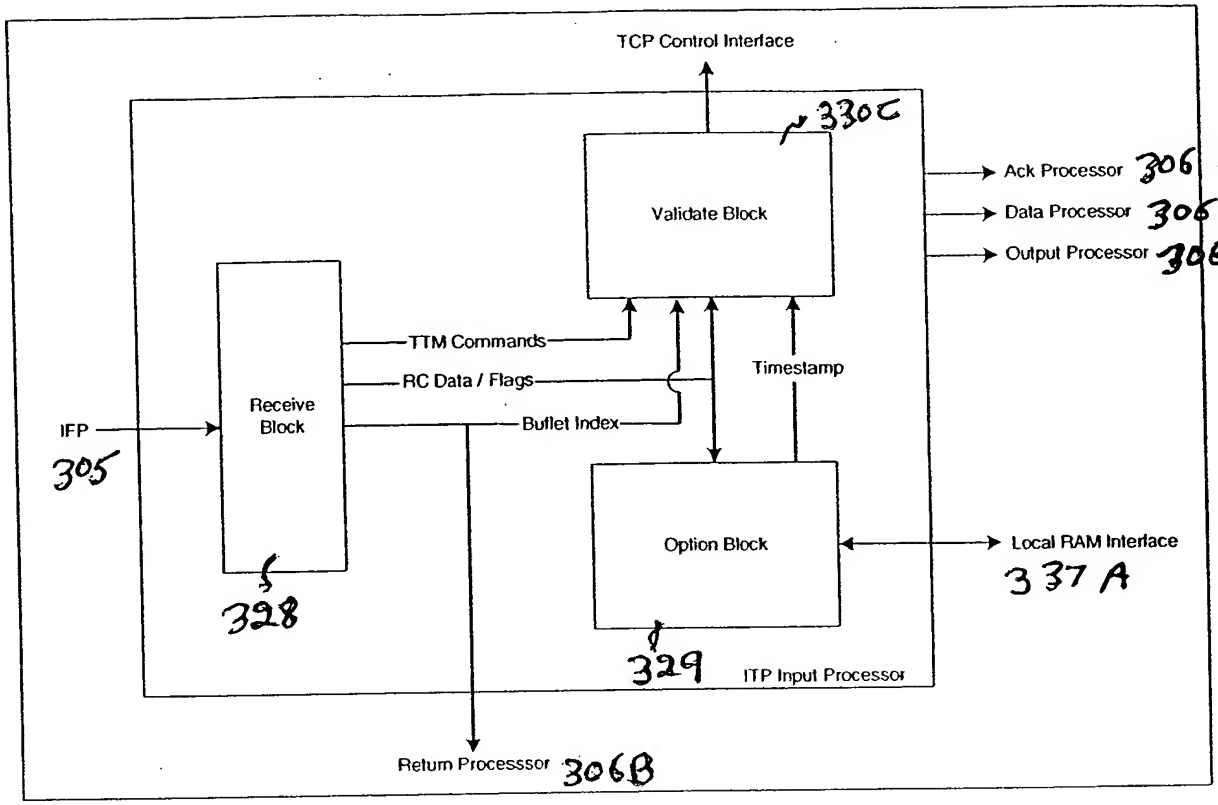


Figure 3C – ITP Input Processor

306A

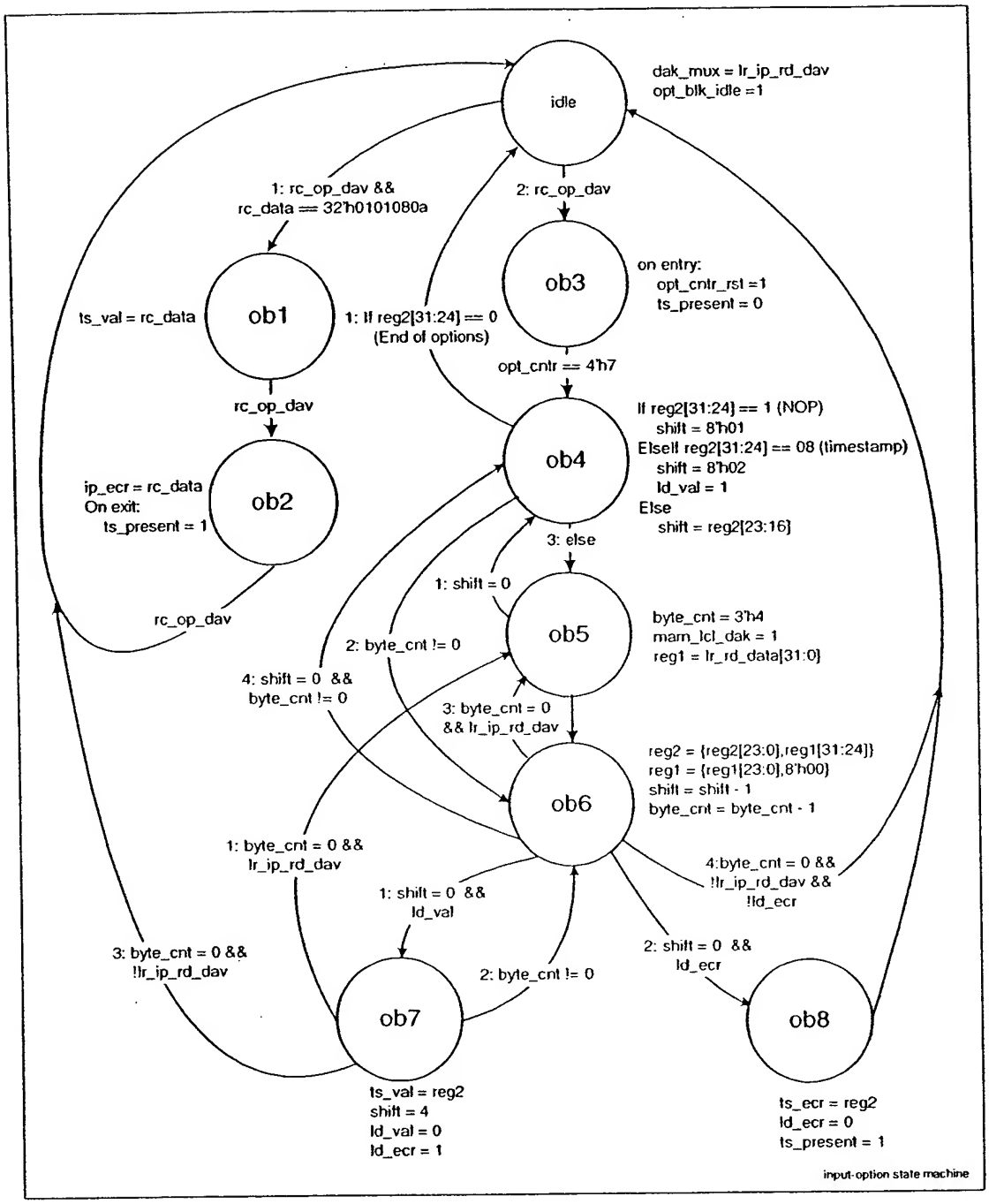


Figure 3C1 Input Processor Option Block State Machine

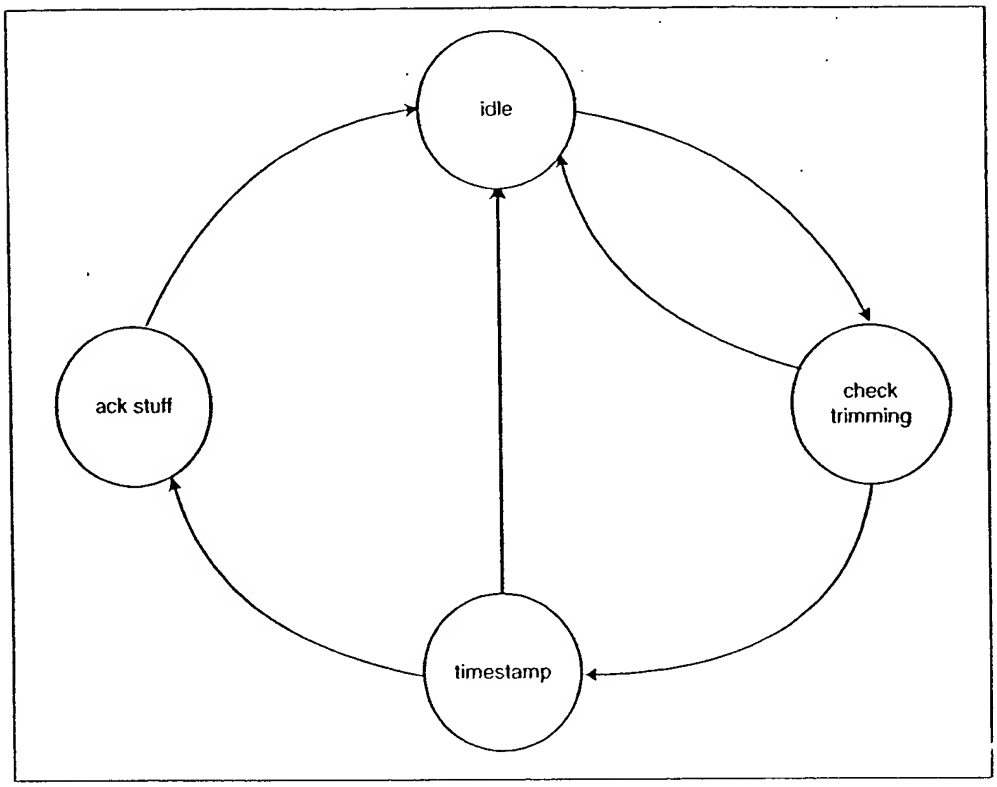


Figure 3C2: Validation State Machine

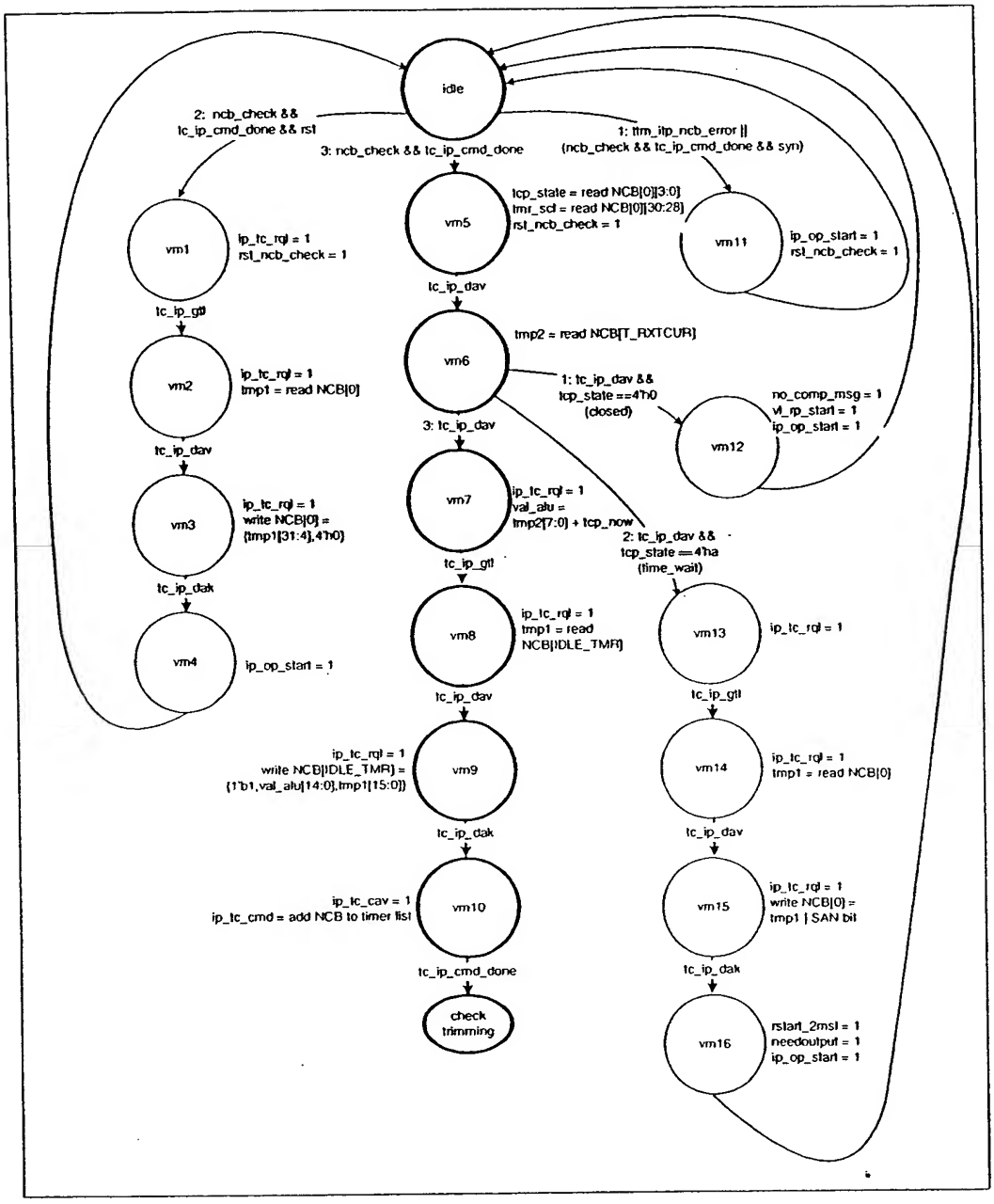


Figure 3C3: Validation State Machine for Reset, SYN or Invalid State

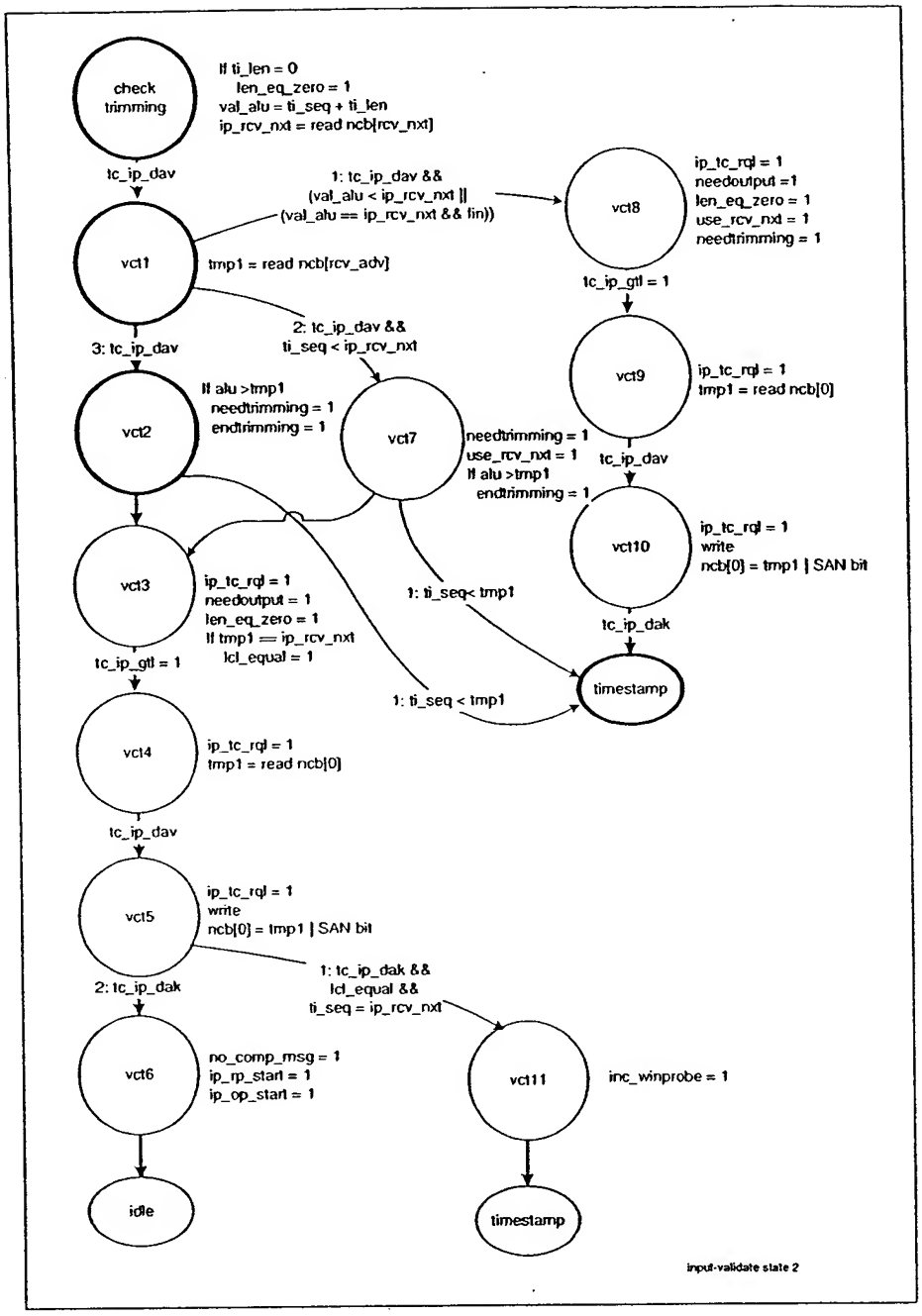


Figure 3C4: Validation State Machine for Trimming

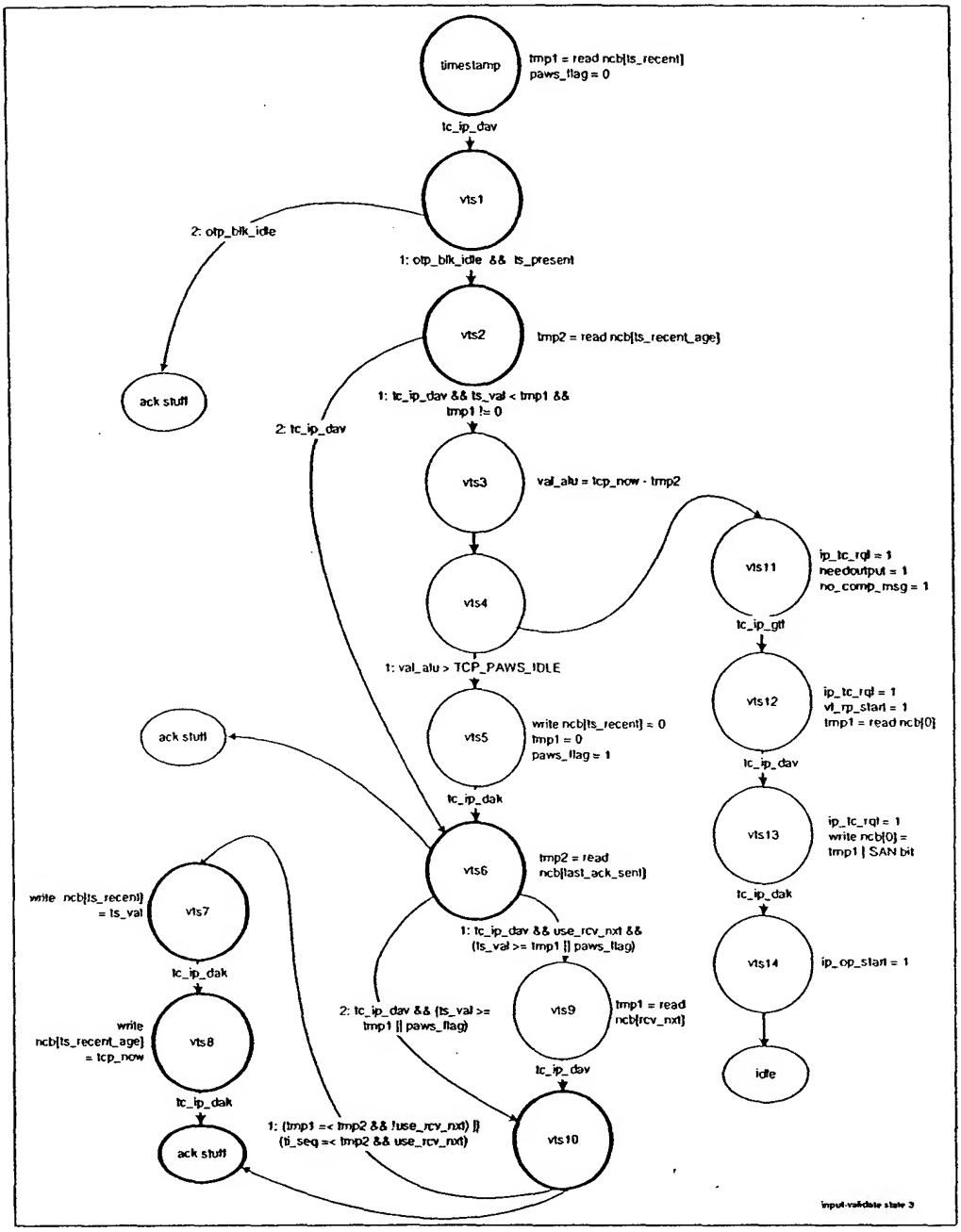


Figure 3C5: Validation State machine for Timestamp functionality

18 of 51

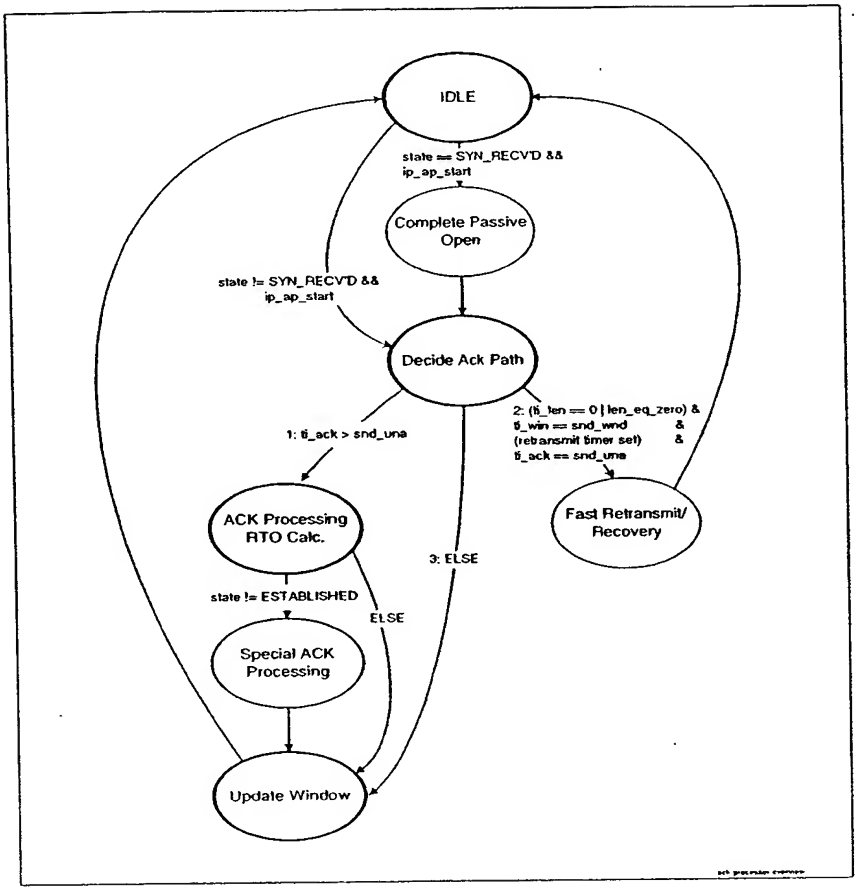


Figure3C6– ACK Processor

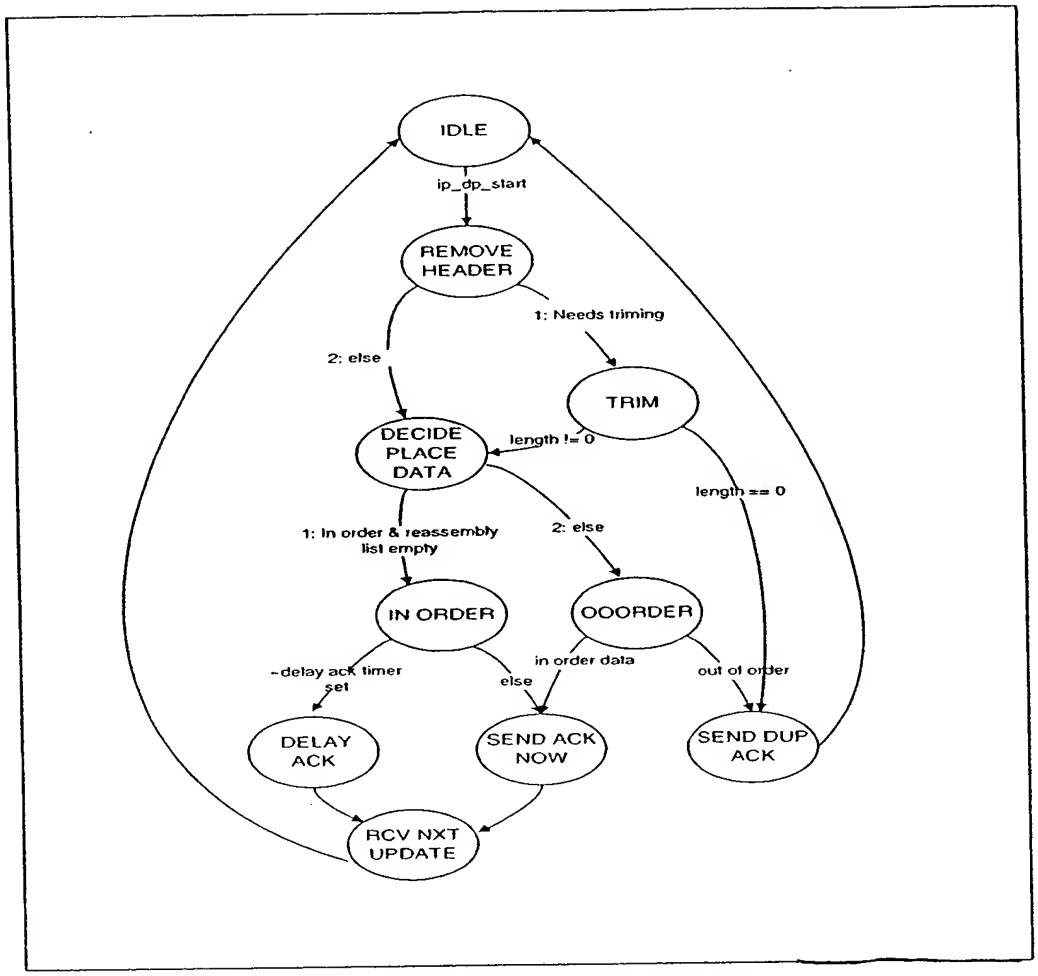


Figure 3C7 Data Processing State Machine

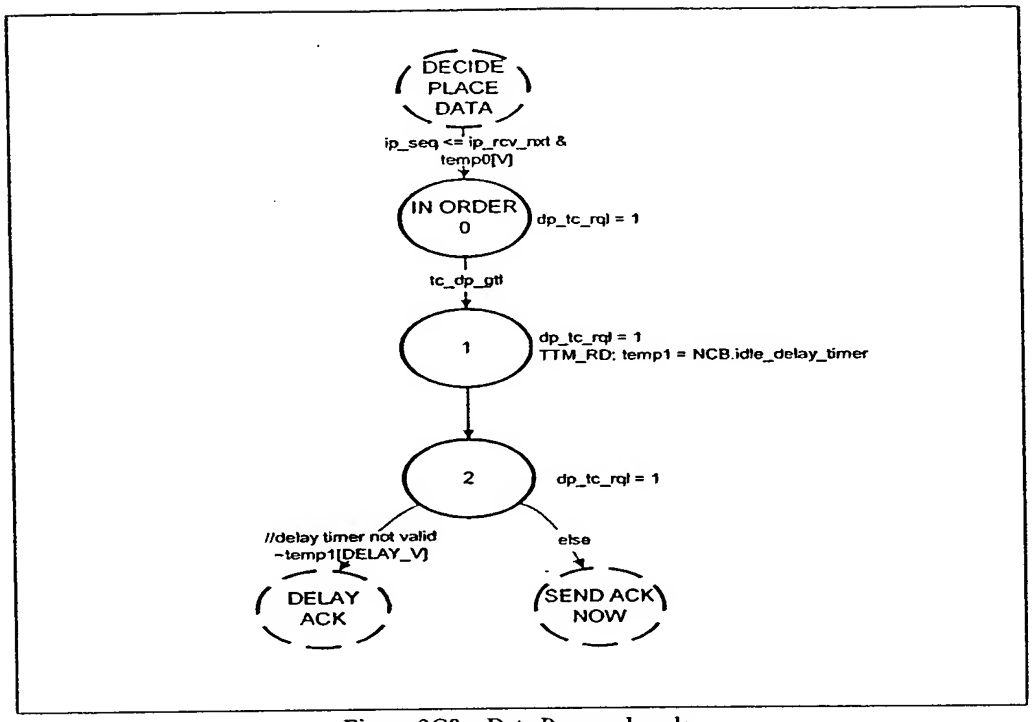


Figure 3C8 – Data Process Inorder

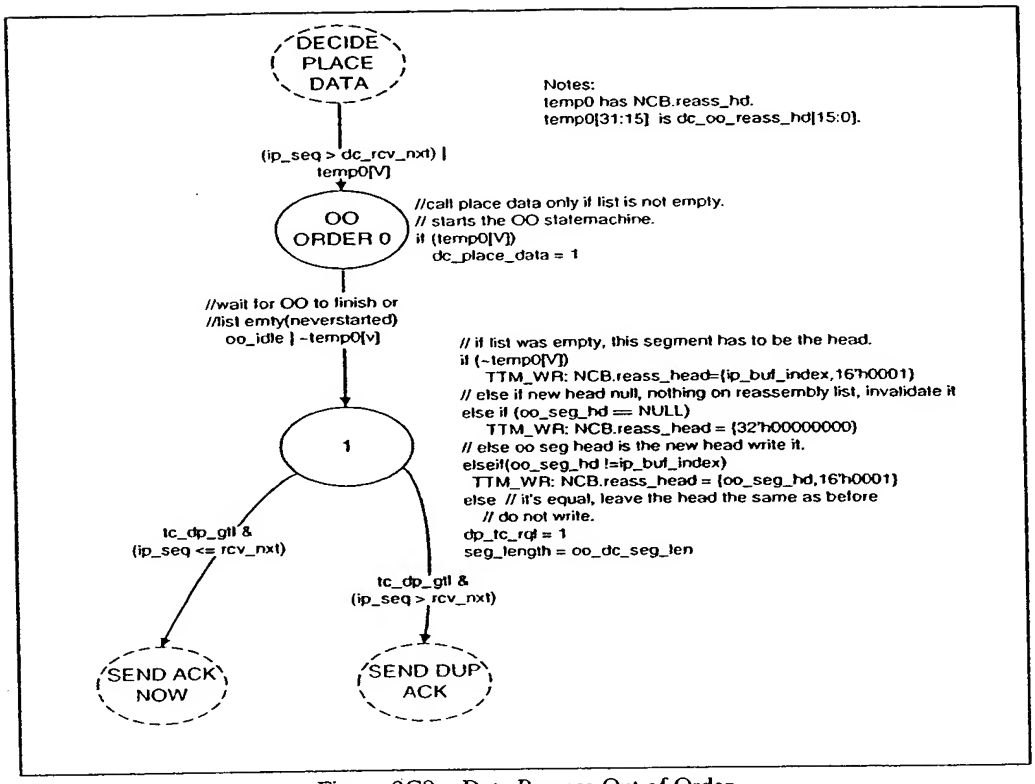


Figure 3C9 – Data Process Out of Order

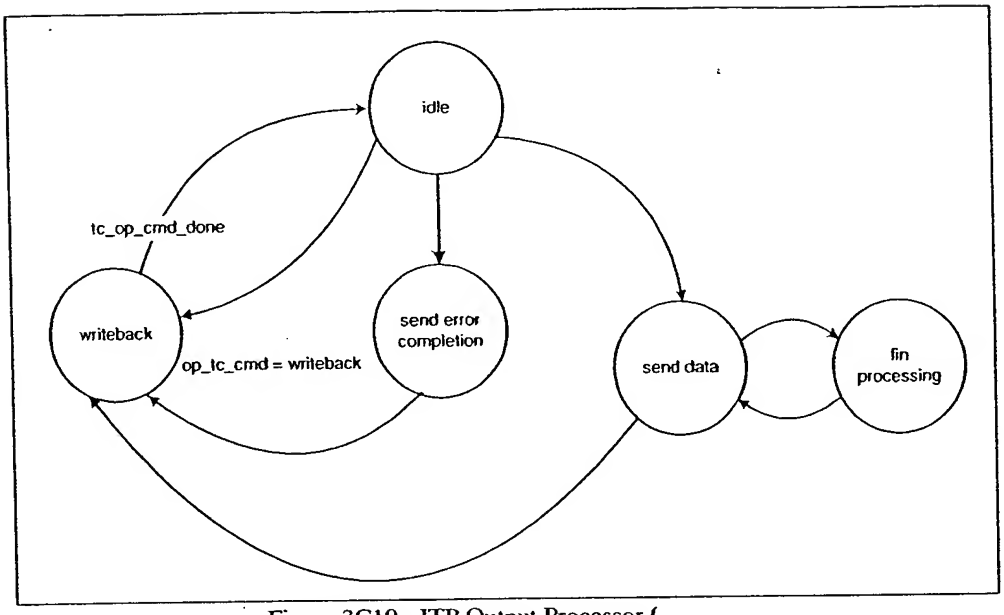


Figure 3C10 - ITP Output Processor (

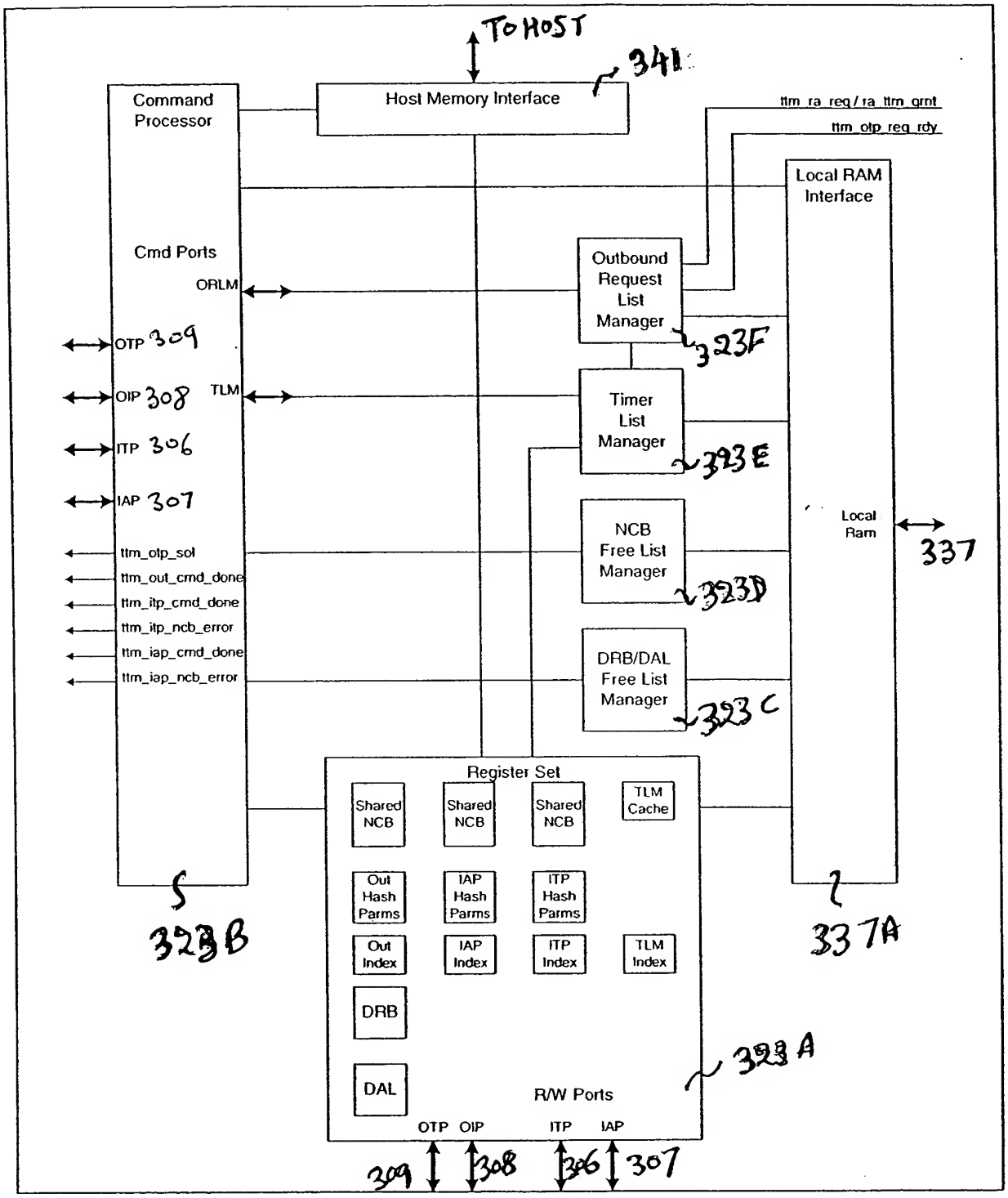


Figure 3D 1

323

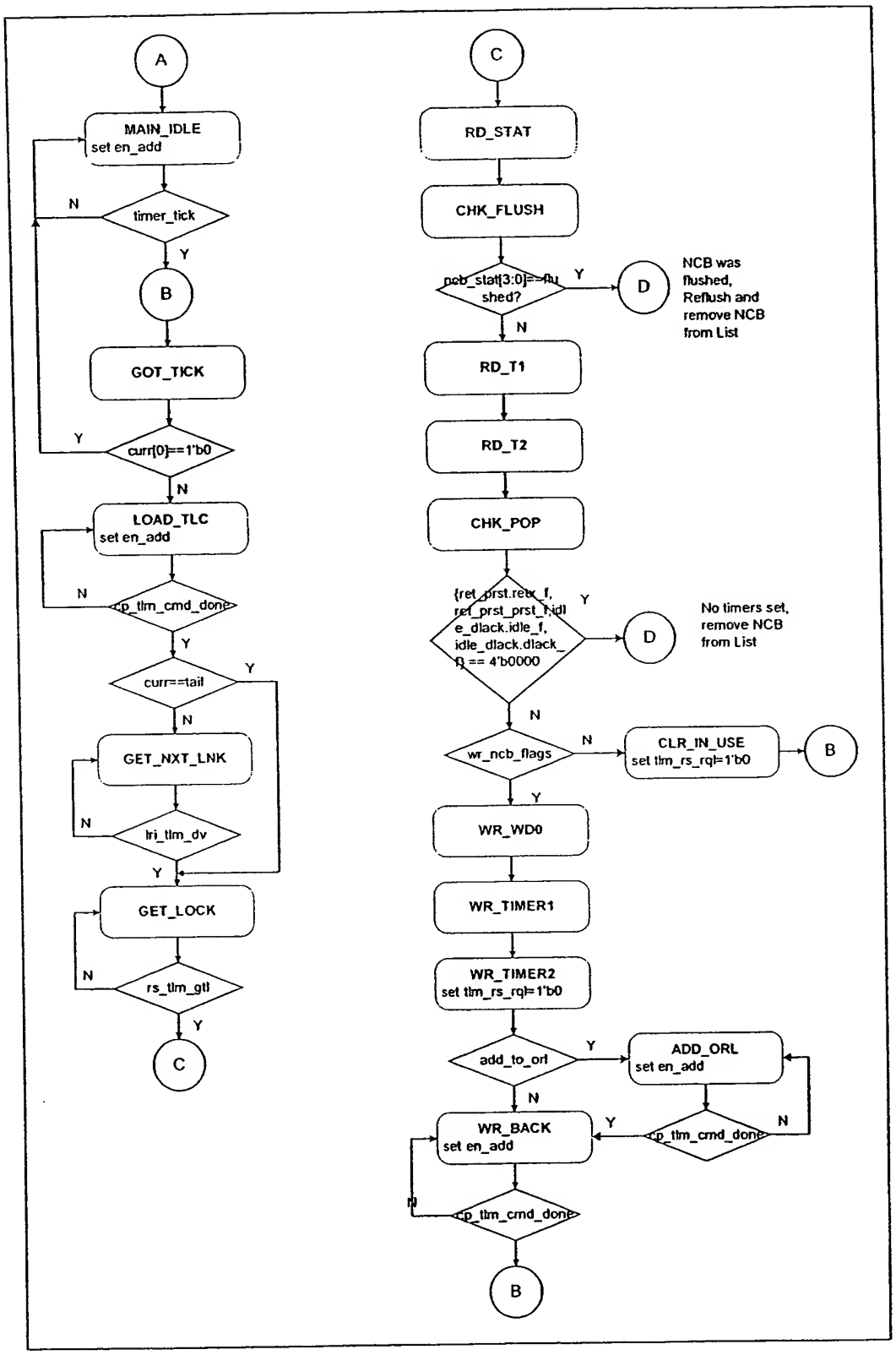


Figure 3D1 Timer List Manager State Machine

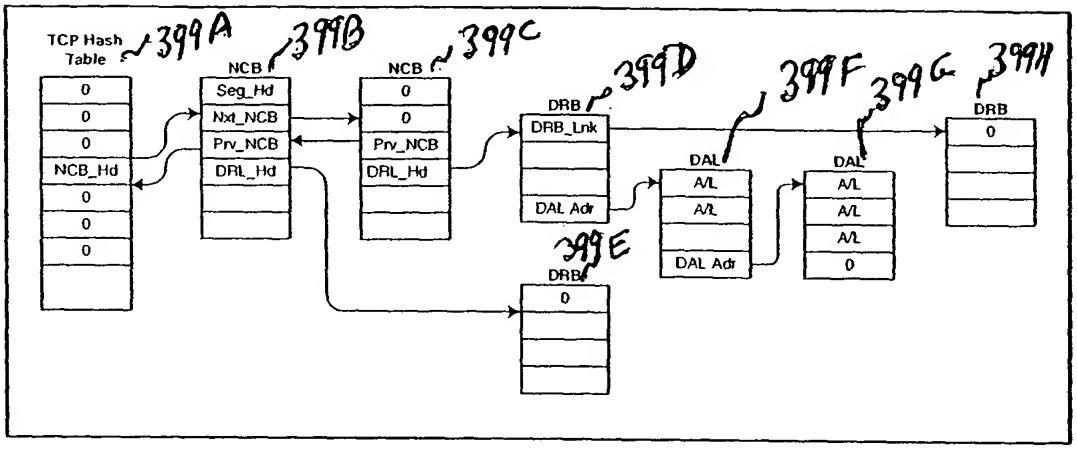


Figure 3E

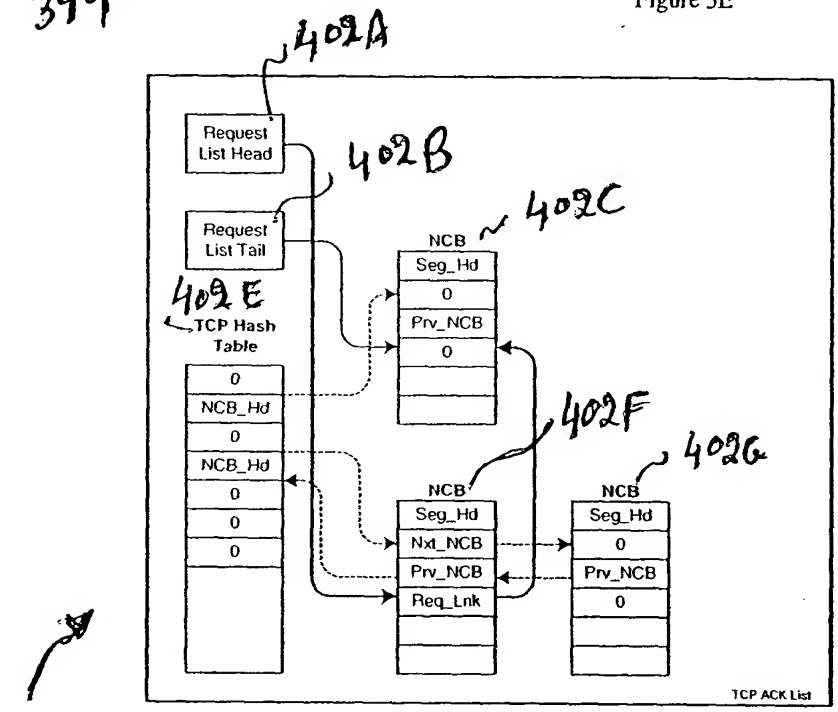


Figure 3F

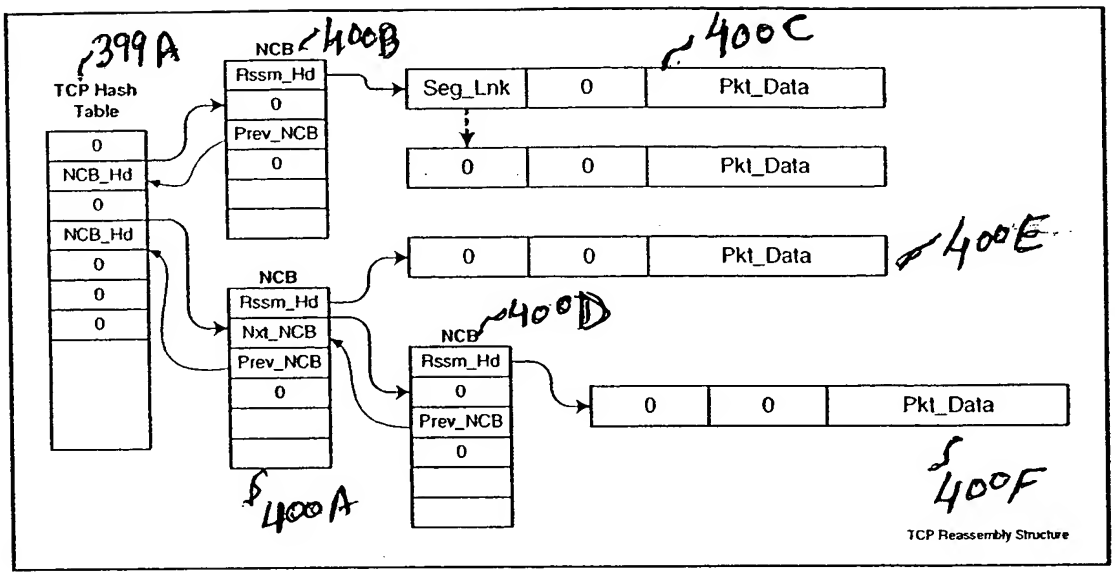


Figure 3G

400

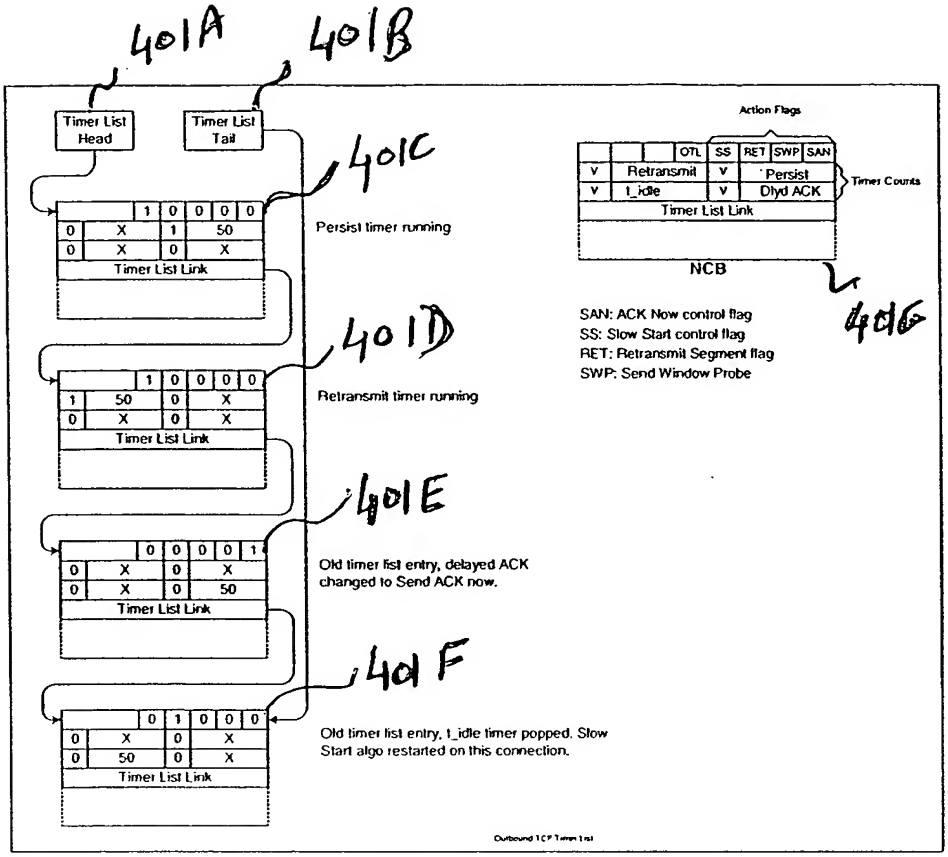


Figure 3H

401

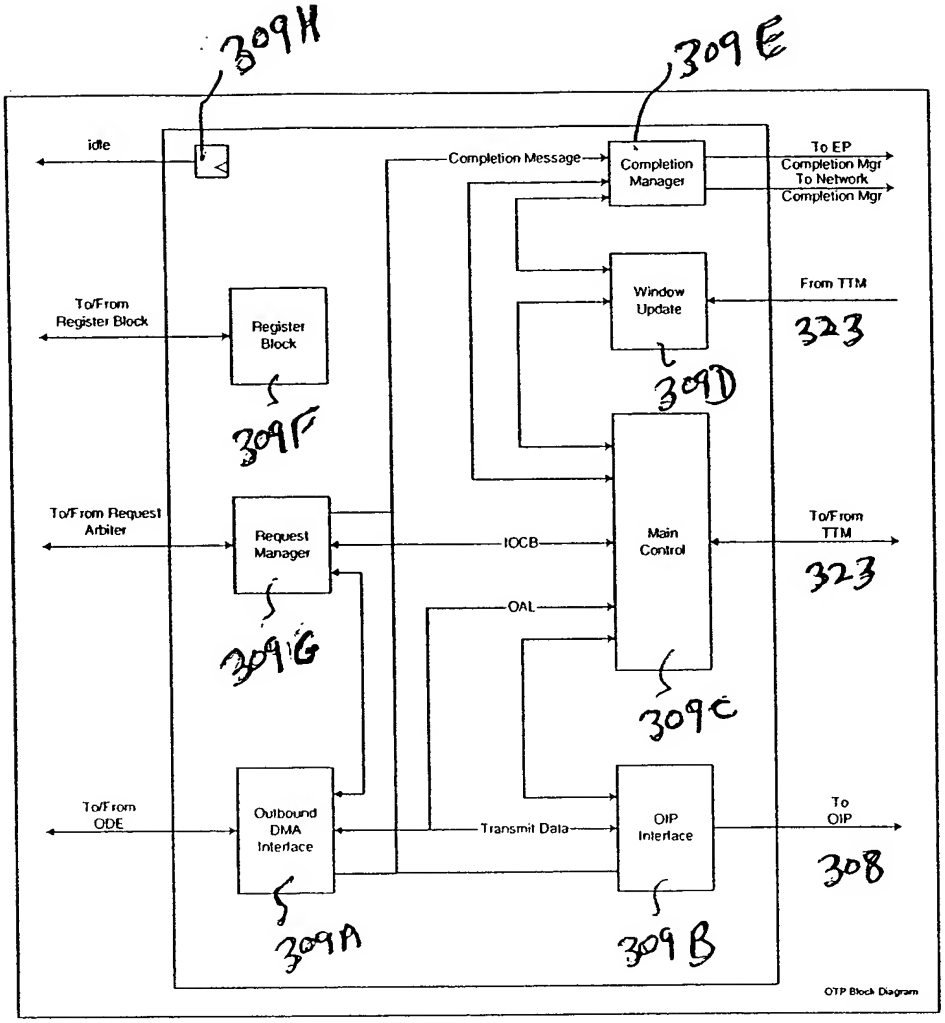


Figure 31

309

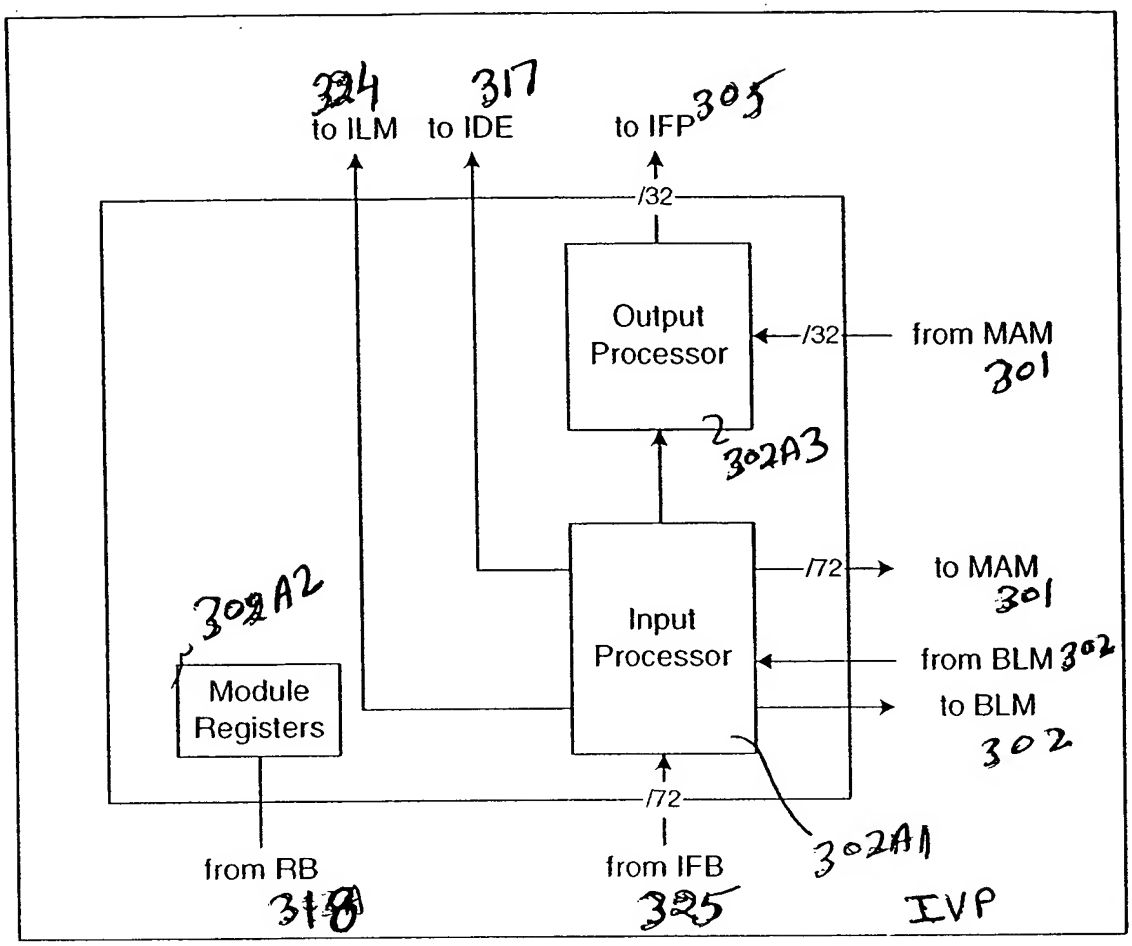


Figure 3J

302A

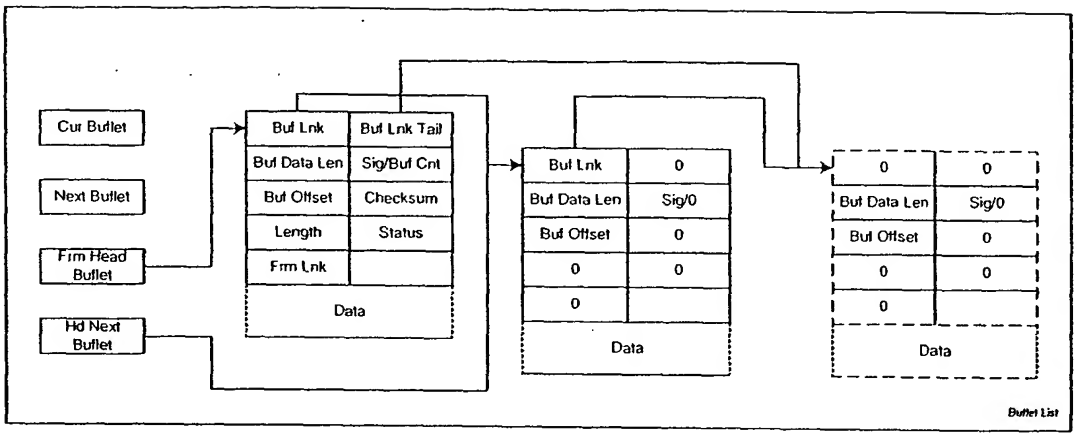


Figure 3J1 Buflet List Structure

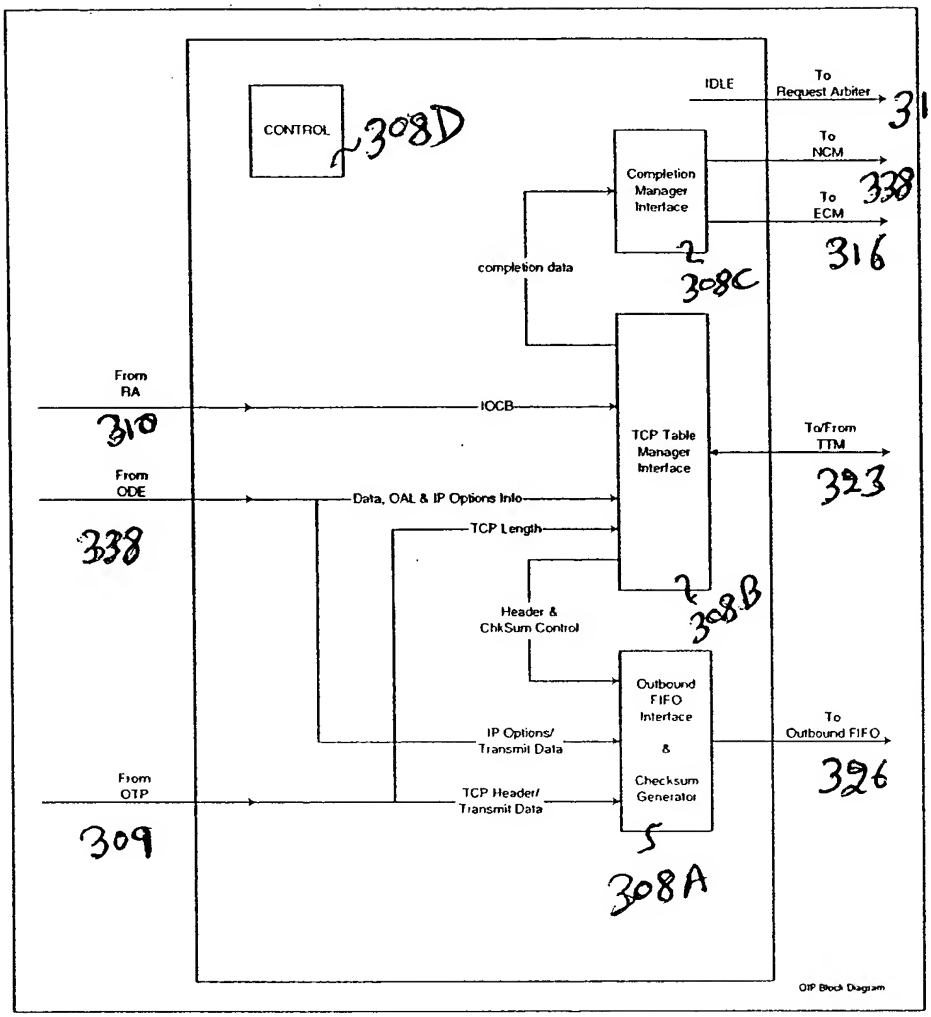


Figure 3K

308

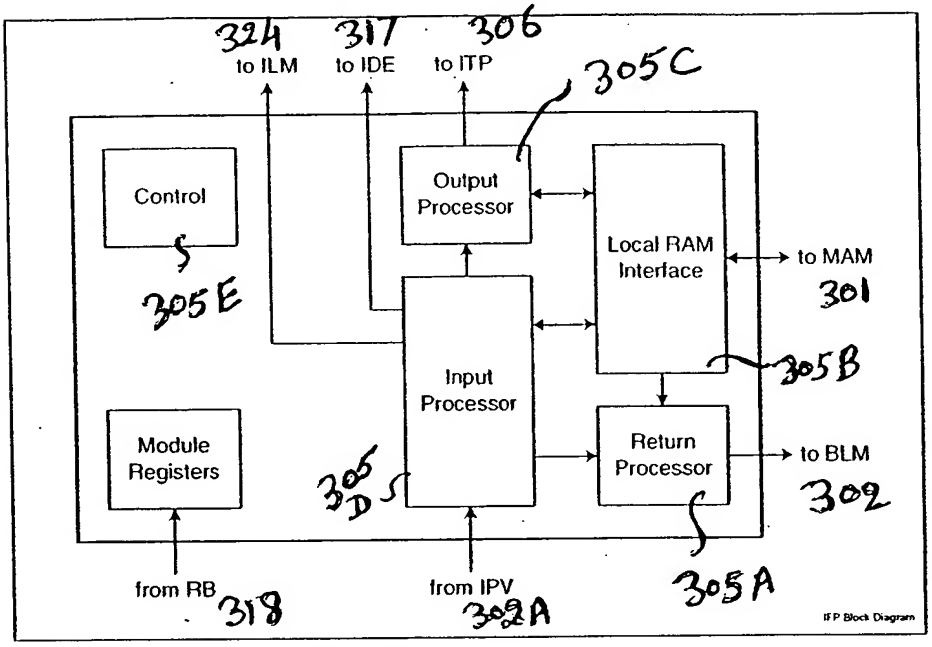


Figure 3L

305

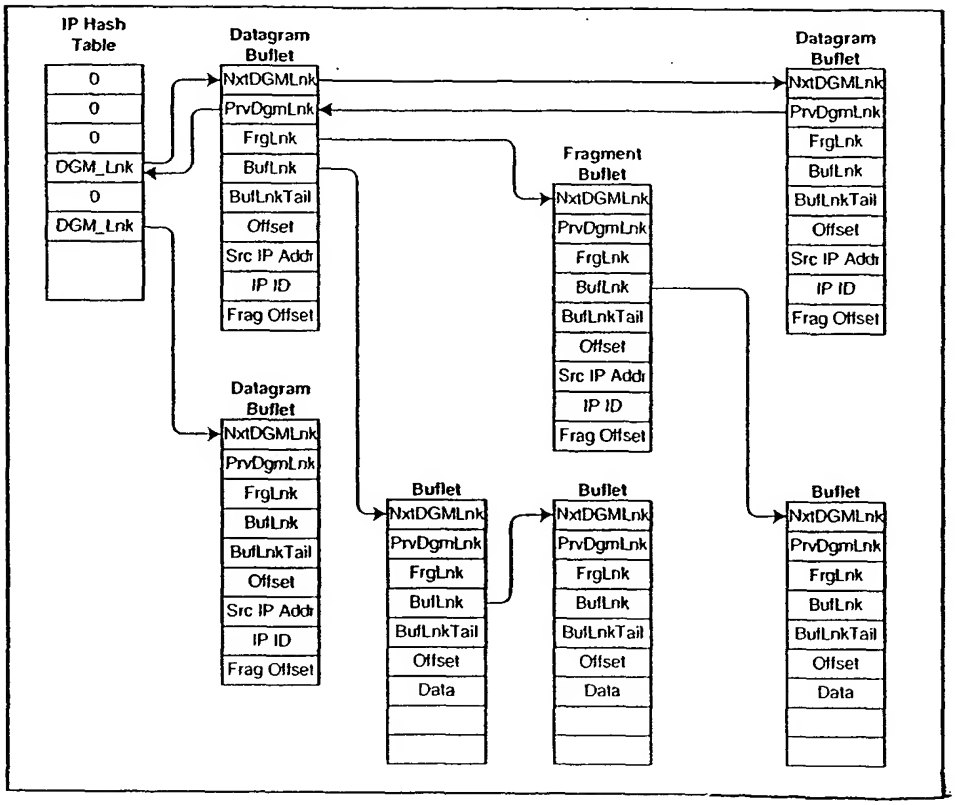

IP Hash Table
0
0
0
DGM_Lnk
0
DGM_Lnk
Datagram Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Src IP Addr
IP ID
Frag Offset
Datagram Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Src IP Addr
IP ID
Frag Offset
Fragment Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Src IP Addr
IP ID
Frag Offset
Datagram Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Src IP Addr
IP ID
Frag Offset
Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Data
Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Data
Buflet
NxtDGMLnk
PrvDgmLnk
FrgLnk
BufLnk
BufLnkTail
Offset
Data

Figure 3L1: "

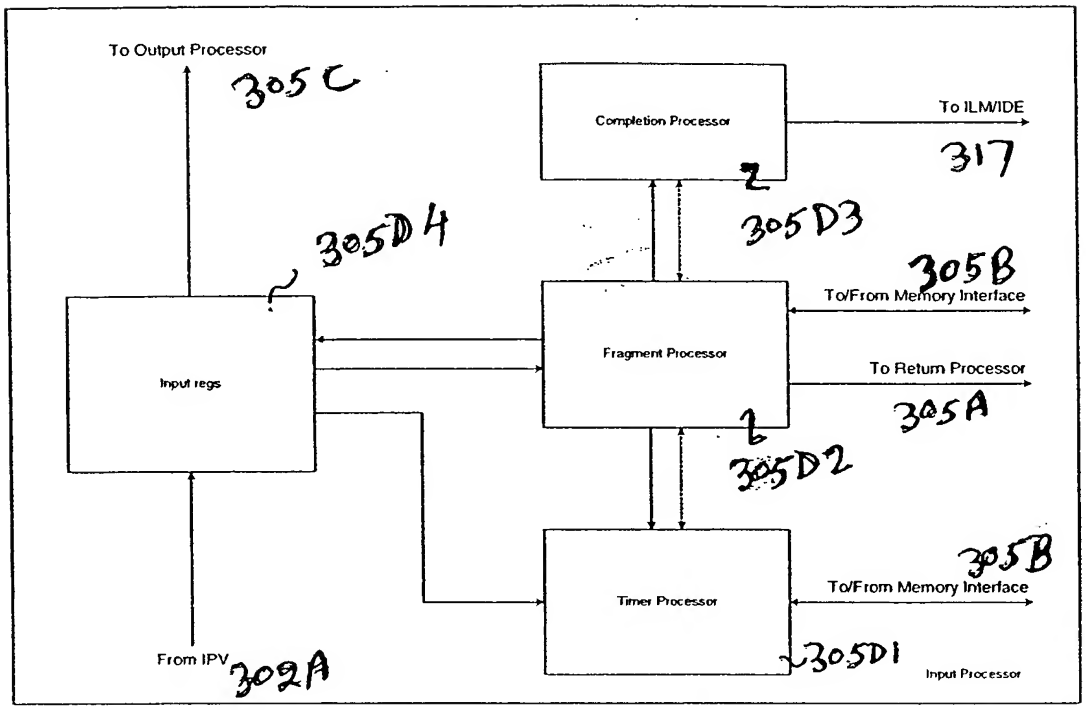


Figure 3L2

305D

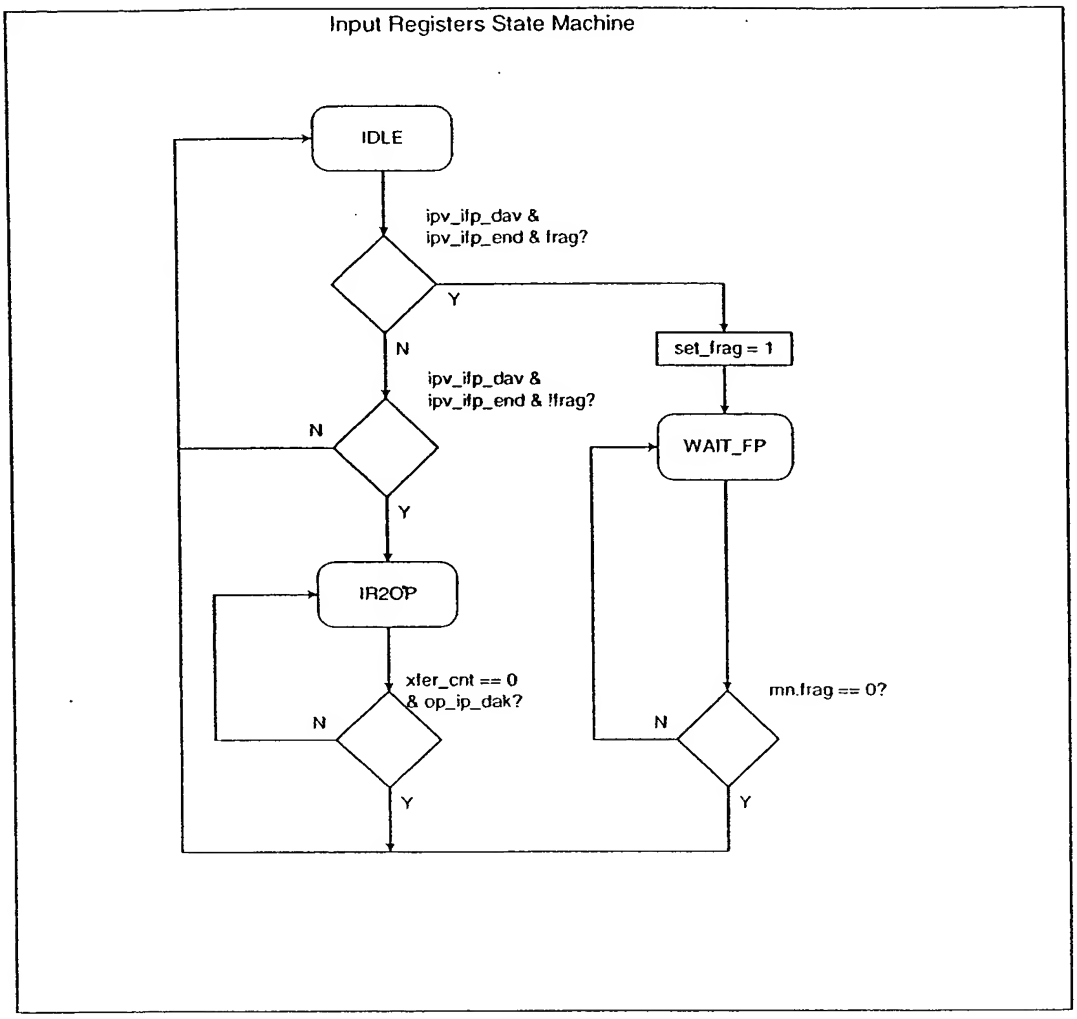

Input Registers State Machine
IDLE
ipv_ifp_dav &
ipv_ifp_end & frag?
Y
N
set_frag = 1
ipv_ifp_dav &
ipv_ifp_end & !frag?
N
WAIT_FP
Y
IR2OP
xfer_cnt == 0
& op_ip_dak?
mn.frag == 0?
N
N
Y
Y

Figure 3L3

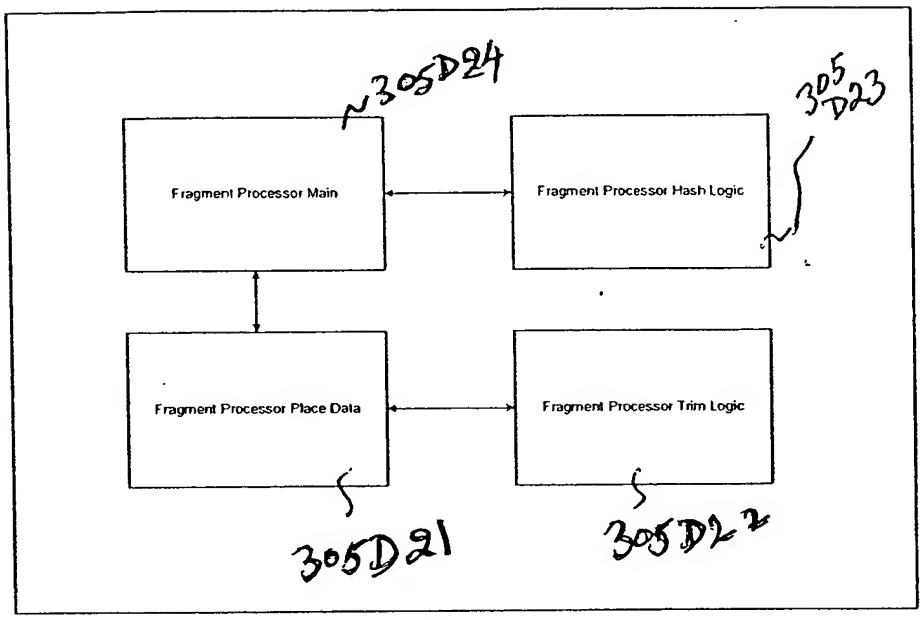


Figure 3L4

305D2

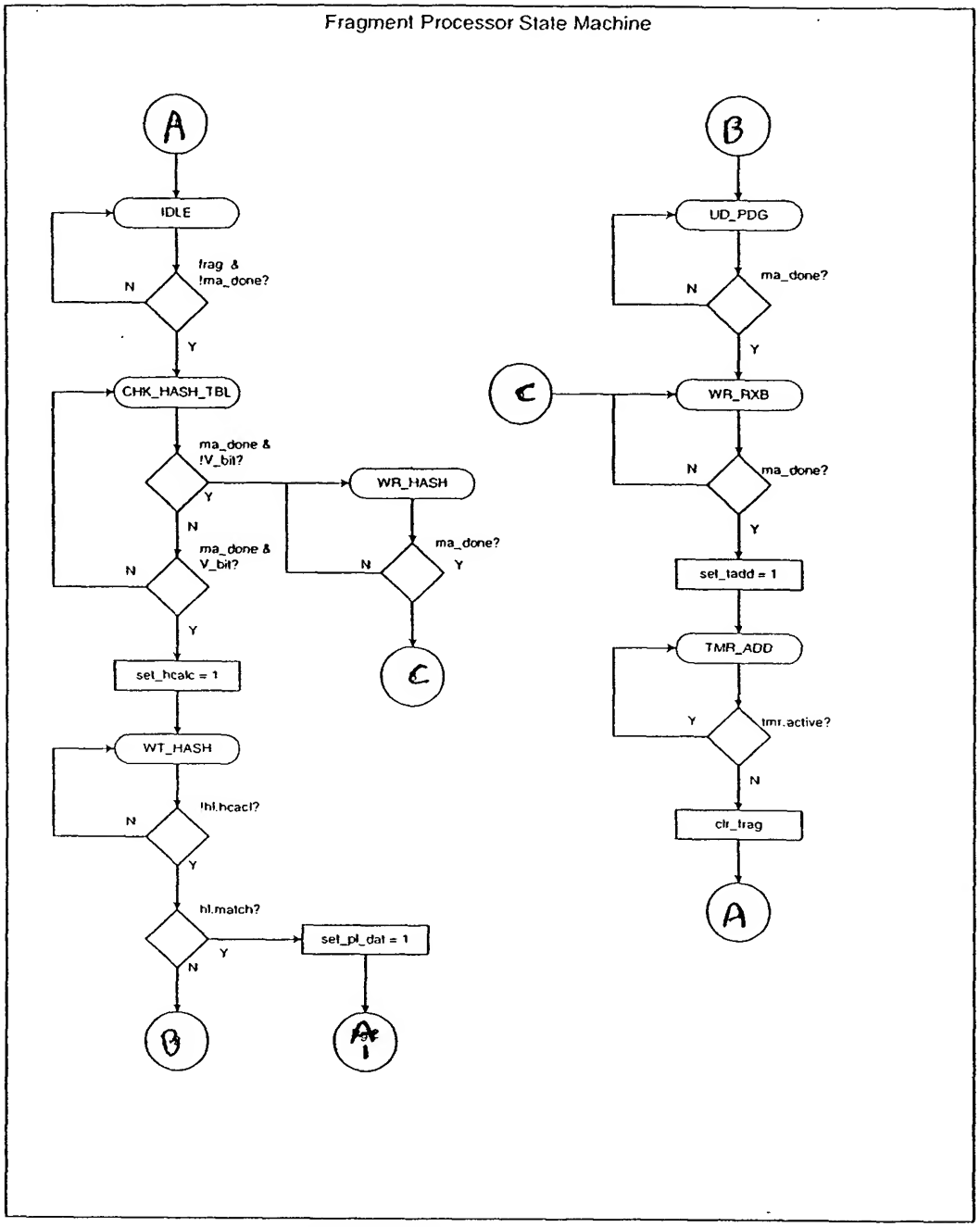


Figure 3L5A I

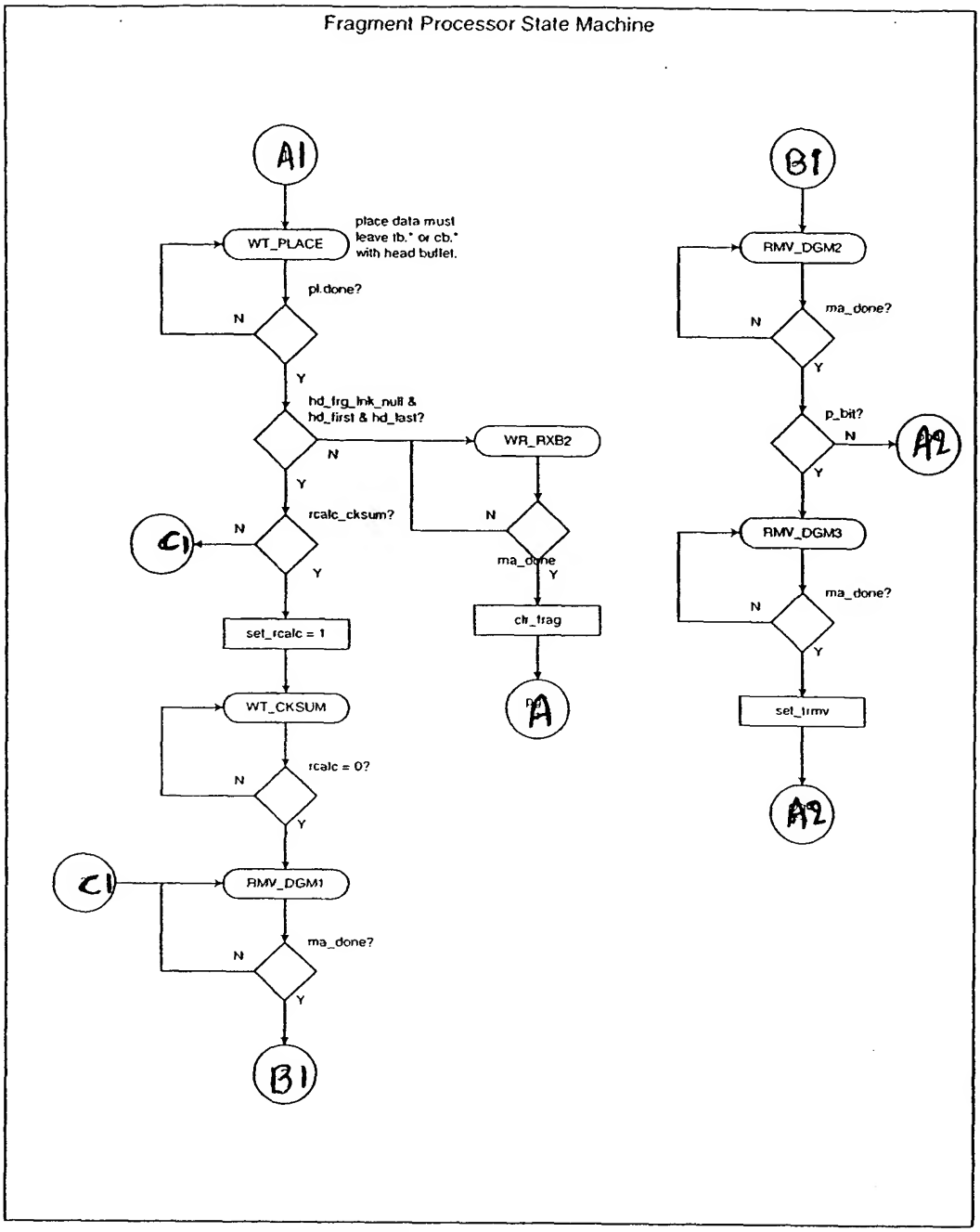


Figure 3L5B F

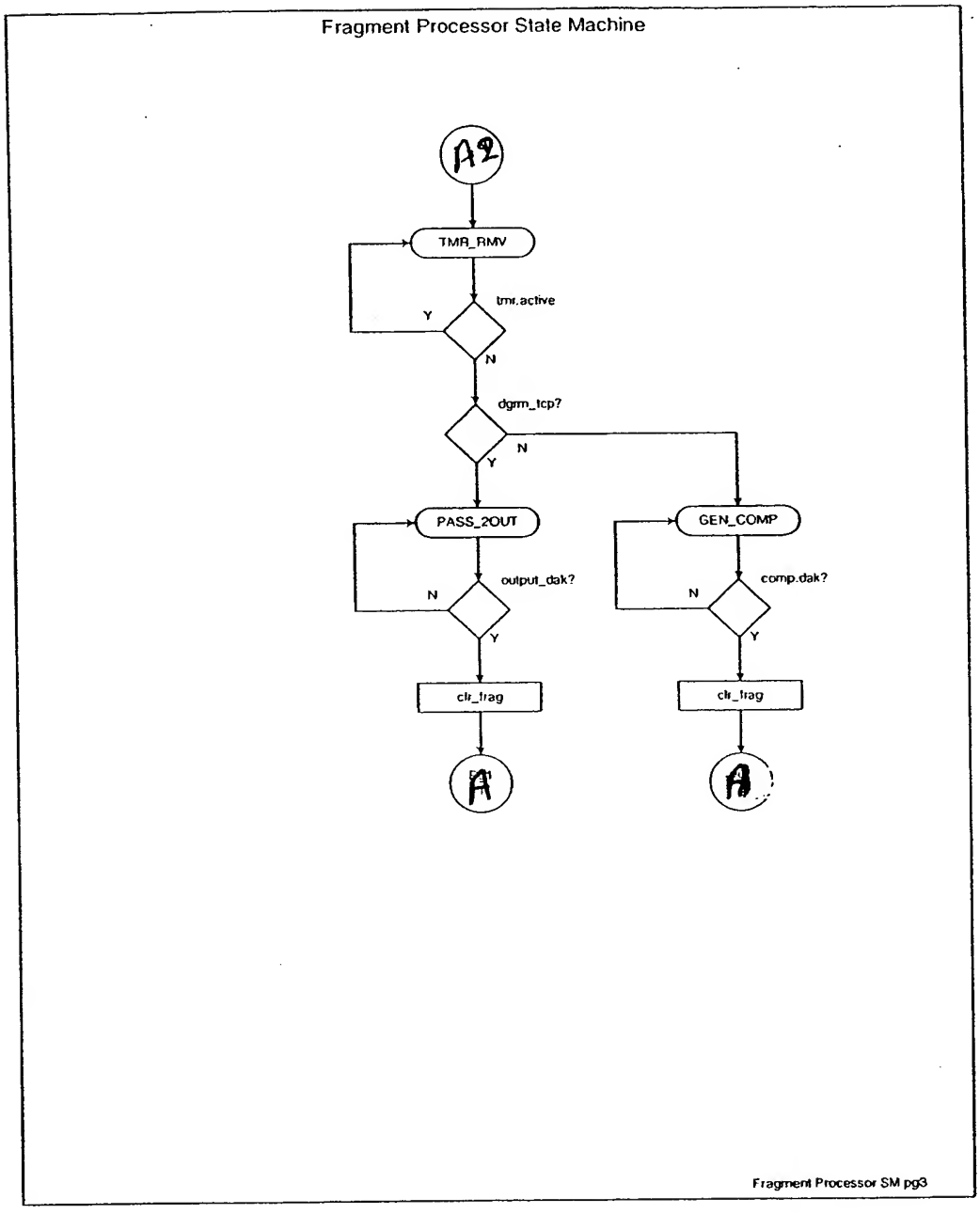

Fragment Processor State Machine
A2
TMR_RMV
tmr.active
Y
N
dgrm_tcp?
Y
N
PASS_2OUT
output_dak?
N
Y
clr_frag
A
GEN_COMP
comp.dak?
N
Y
clr_frag
A
Fragment Processor SM pg3

Figure 3L5C

40-651

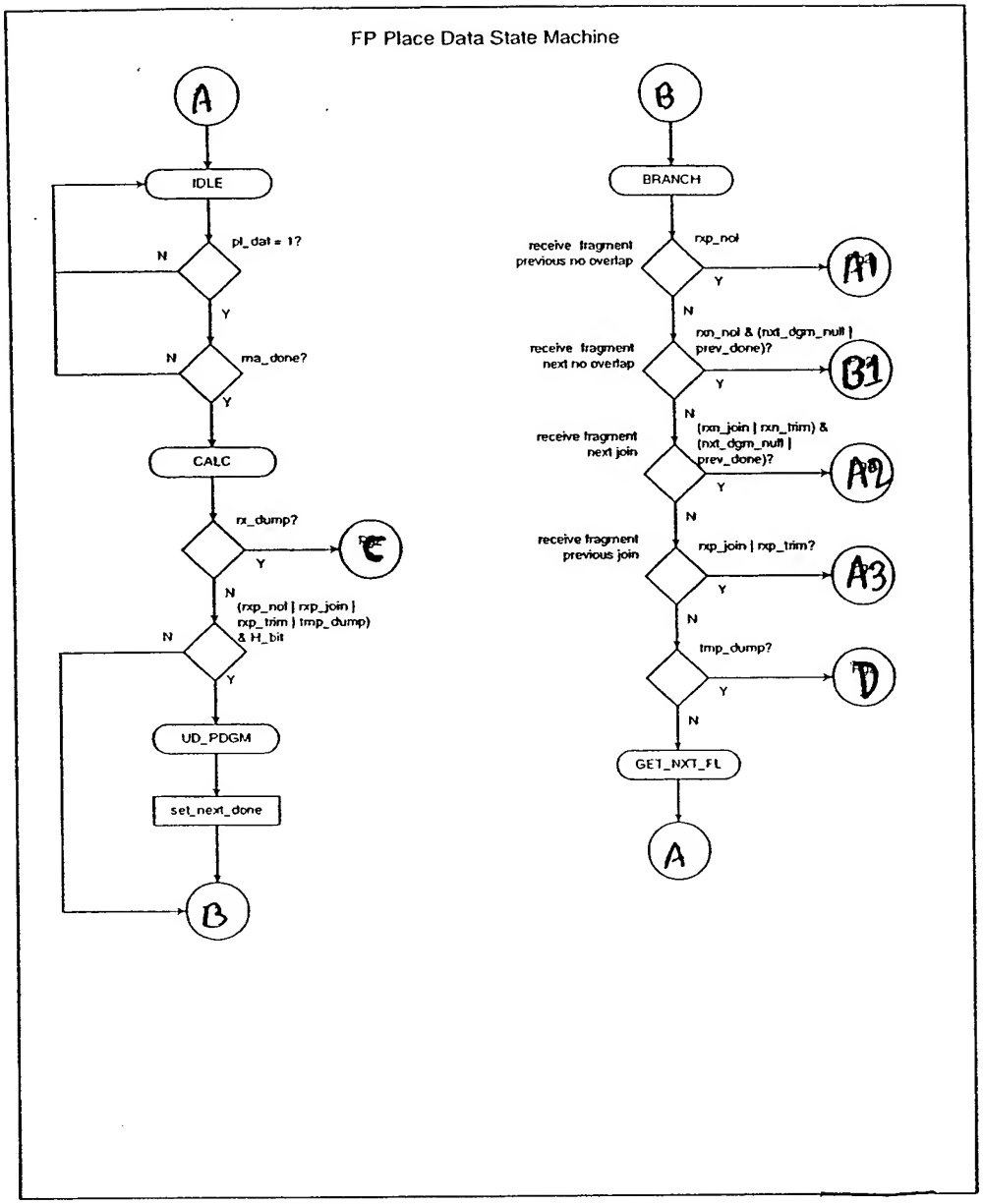


Figure 3L6A

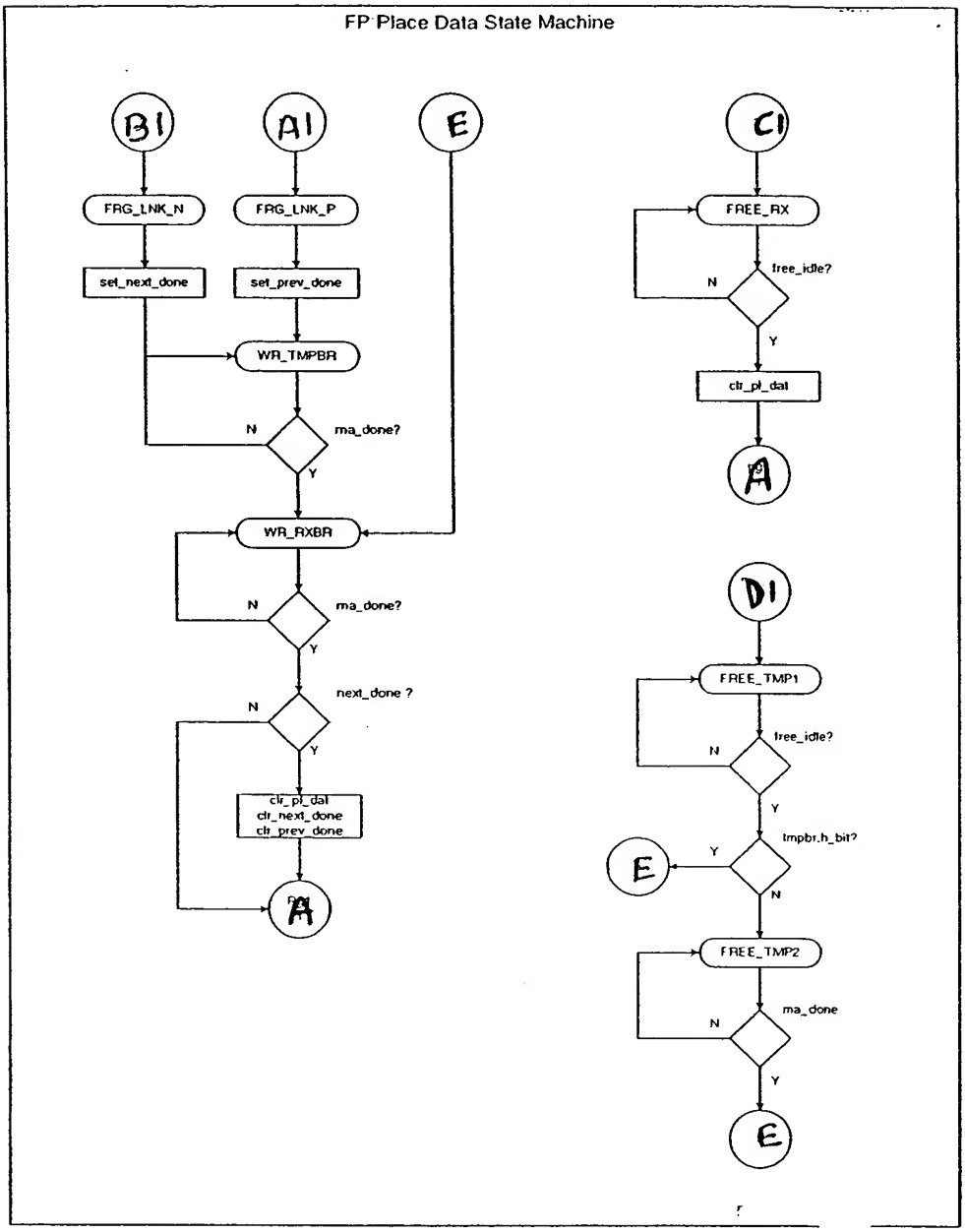

FP Place Data State Machine
B1
A1
E
C1
FRG_LNK_N
FRG_LNK_P
FREE_RX
set_next_done
set_prev_done
free_idle?
N
Y
WR_TMPBR
clr_pl_dat
N
rma_done?
Y
A
WR_RXBR
D1
N
rma_done?
Y
FREE_TMP1
N
next_done ?
free_idle?
Y
clr_pl_dat
clr_next_done
clr_prev_done
Y
tmpbr.h_bit?
E
N
A
FREE_TMP2
rma_done
N
Y
E

Figure 3L6 B

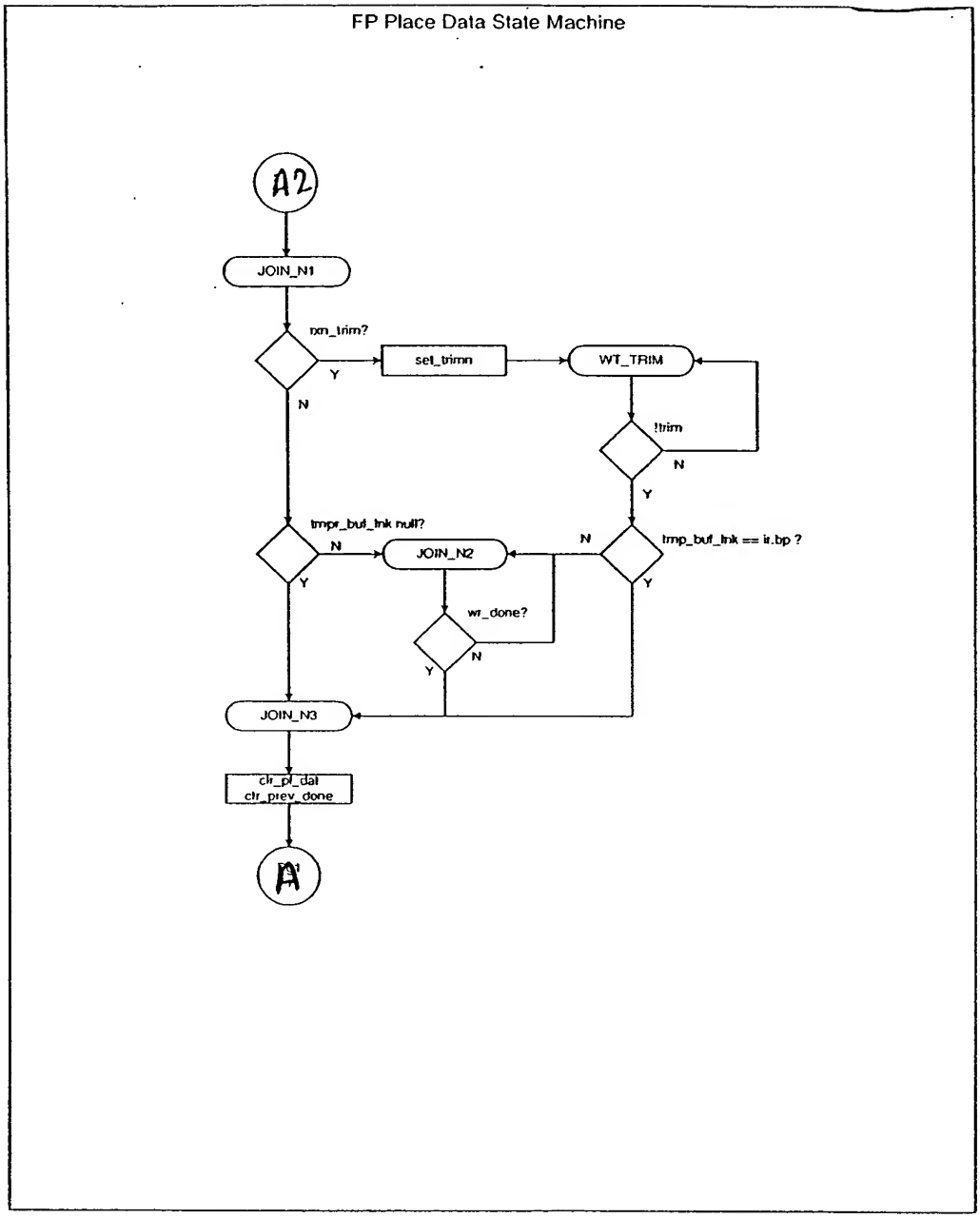

FP Place Data State Machine
A2
JOIN_N1
txn_trim?
Y
N
set_trimn
WT_TRIM
!trim
N
Y
tmpr_buf_lnk null?
N
Y
JOIN_N2
N
tmp_buf_lnk == ir.bp ?
Y
wr_done?
Y
N
JOIN_N3
clr_pf_dat
clr_prev_done
A1

Figure 3L6C

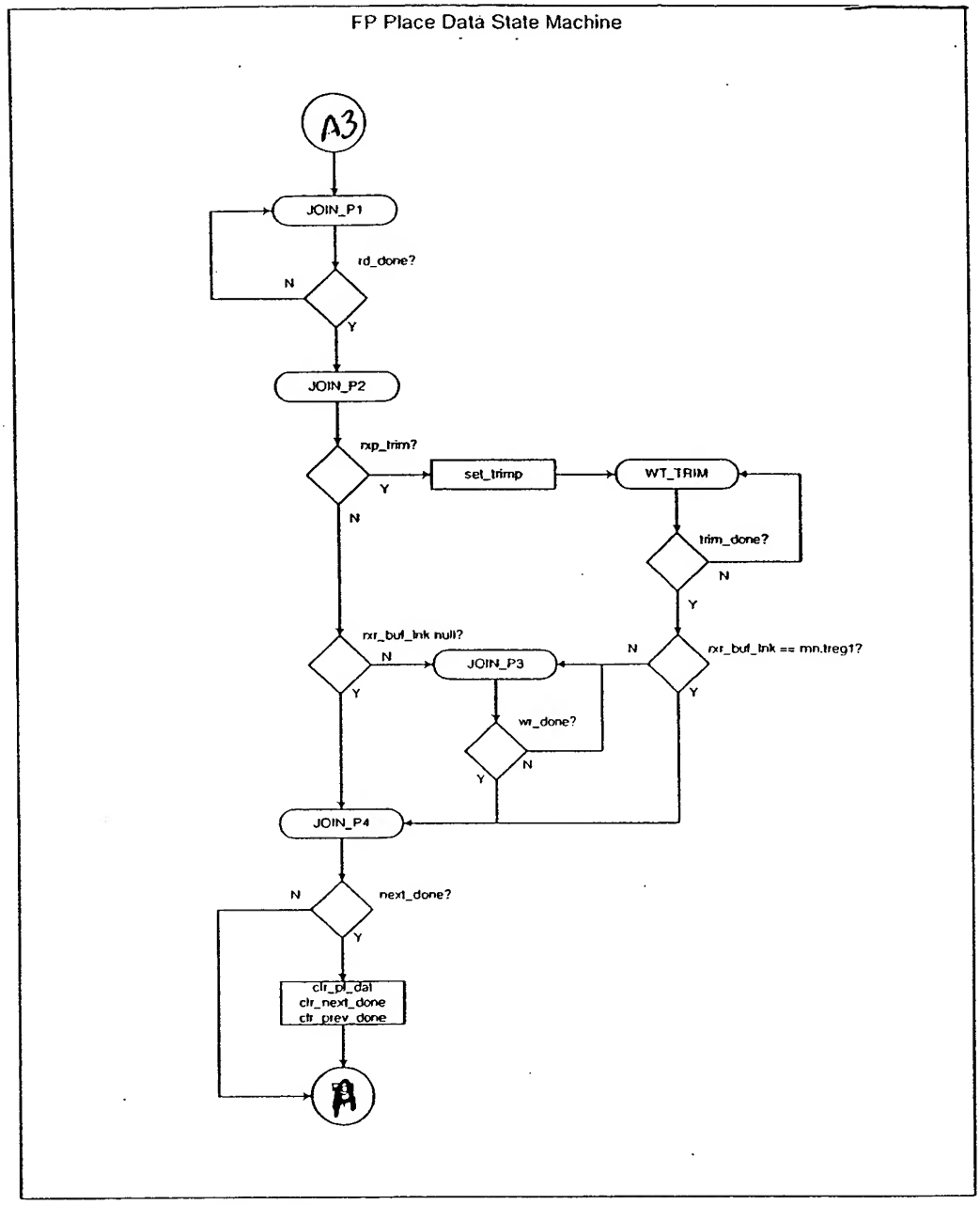

FP Place Data State Machine
A3
JOIN_P1
rd_done?
N
Y
JOIN_P2
rxp_trim?
Y
set_trimp
WT_TRIM
N
trim_done?
N
Y
rxr_buf_lnk null?
N
JOIN_P3
N
rxr_buf_lnk == mn.treg1?
Y
Y
wr_done?
N
Y
JOIN_P4
N
next_done?
Y
clr_pl_dat
clr_next_done
clr_prev_done
A

Figure 3L6D

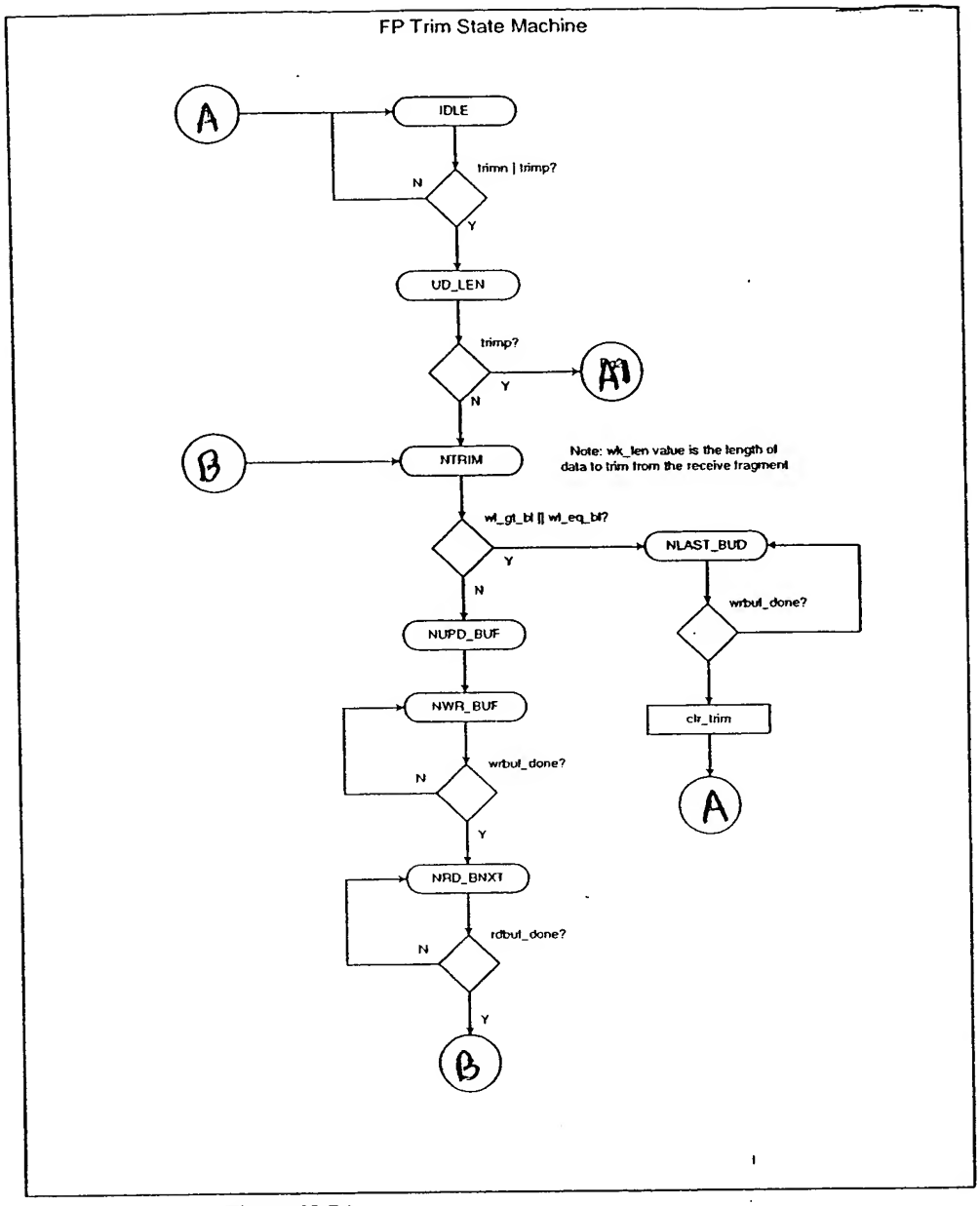

FP Trim State Machine
A
IDLE
trimn | trimp?
N
Y
UD_LEN
trimp?
Y
N
A1
B
NTRIM
Note: wk_len value is the length of data to trim from the receive fragment
wl_gt_bl || wl_eq_bl?
Y
N
NLAST_BUD
wrbuf_done?
NUPD_BUF
NWR_BUF
clr_trim
wrbuf_done?
N
Y
A
NRD_BNXT
rdbuf_done?
N
Y
B

Figure 3L7A

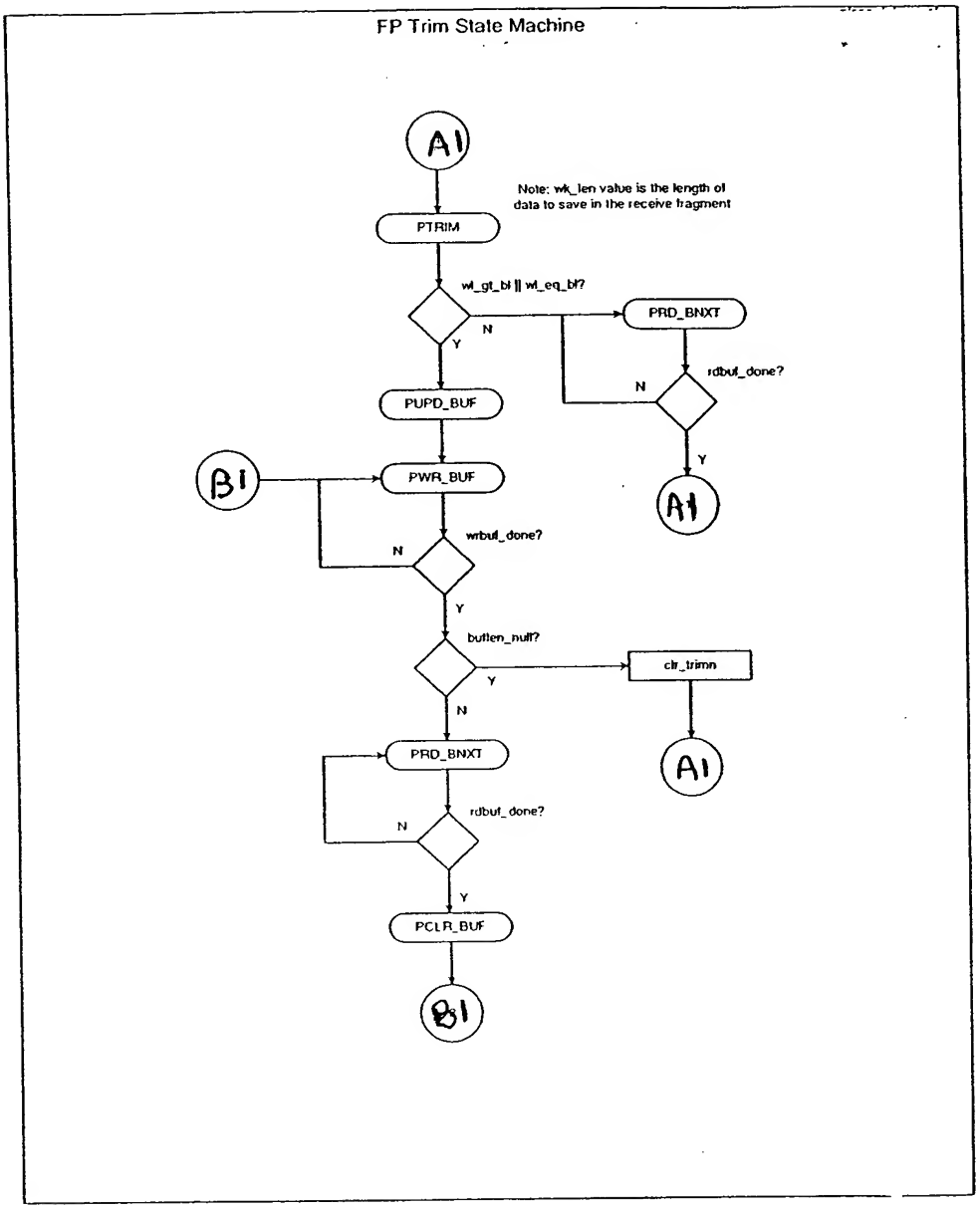

FP Trim State Machine
A1
Note: wk_len value is the length of data to save in the receive fragment
PTRIM
wl_gt_bl || wl_eq_bl?
N
Y
PRD_BNXT
rdbuf_done?
N
Y
A1
PUPD_BUF
B1
PWR_BUF
wrbuf_done?
N
Y
buflen_null?
Y
clr_trimn
N
A1
PRD_BNXT
rdbuf_done?
N
Y
PCLR_BUF
B1

Figure 3L7B:

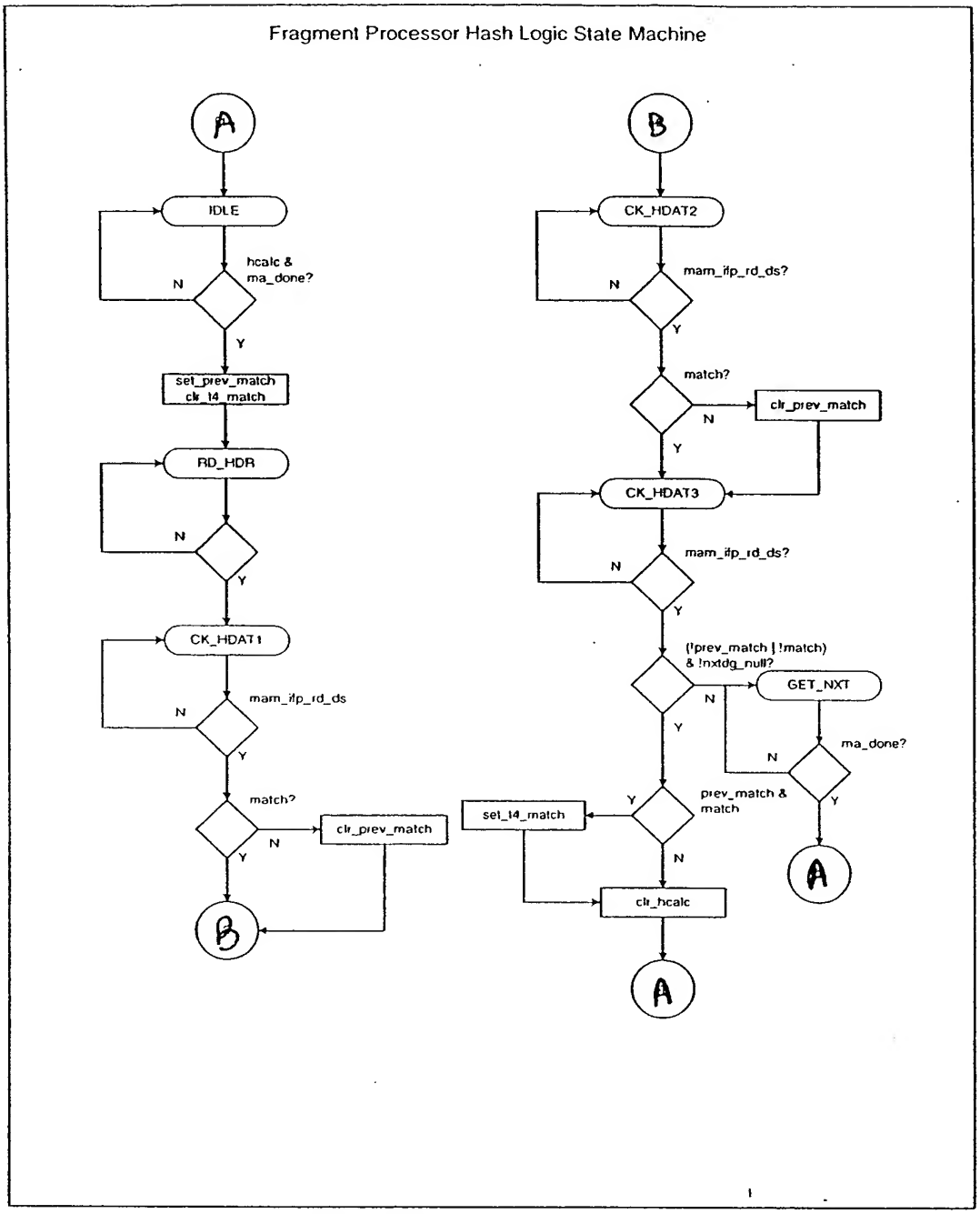

Fragment Processor Hash Logic State Machine
A
IDLE
hcalc &
ma_done?
N
Y
set_prev_match
clr_l4_match
RD_HDR
N
Y
CK_HDAT1
mam_ifp_rd_ds
N
Y
match?
clr_prev_match
N
Y
B
B
CK_HDAT2
mam_ifp_rd_ds?
N
Y
match?
clr_prev_match
N
Y
CK_HDAT3
mam_ifp_rd_ds?
N
Y
(!prev_match | !match)
& !nxtdg_null?
GET_NXT
N
Y
ma_done?
N
Y
prev_match &
match
Y
set_l4_match
N
clr_hcalc
A
A

Figure 3L8 J

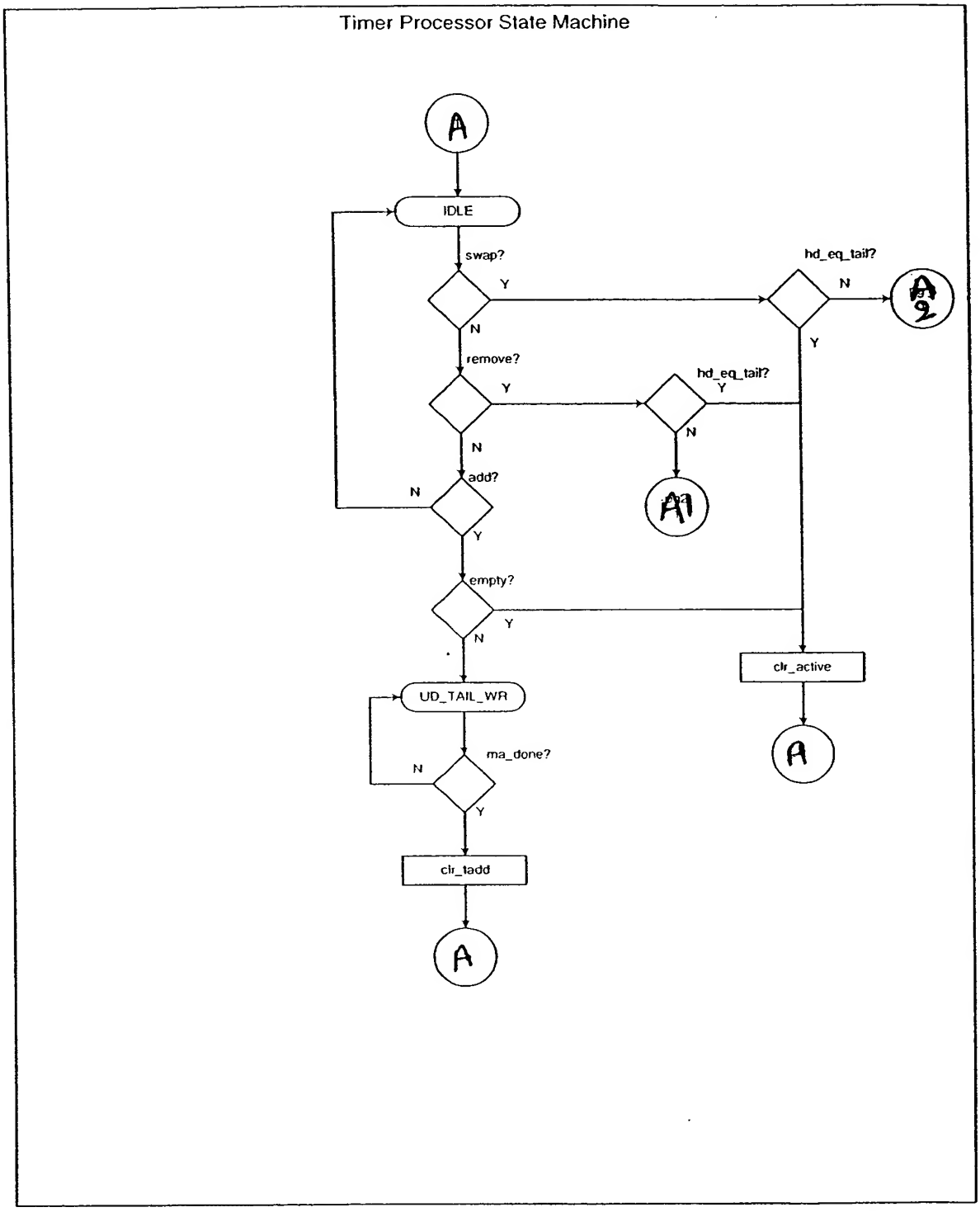

Timer Processor State Machine
A
IDLE
swap?
Y
N
hd_eq_tail?
N
Y
A2
remove?
Y
hd_eq_tail?
Y
N
N
add?
N
Y
A1
empty?
Y
N
clr_active
UD_TAIL_WR
ma_done?
N
Y
A
clr_tadd
A

Figure 3L9A

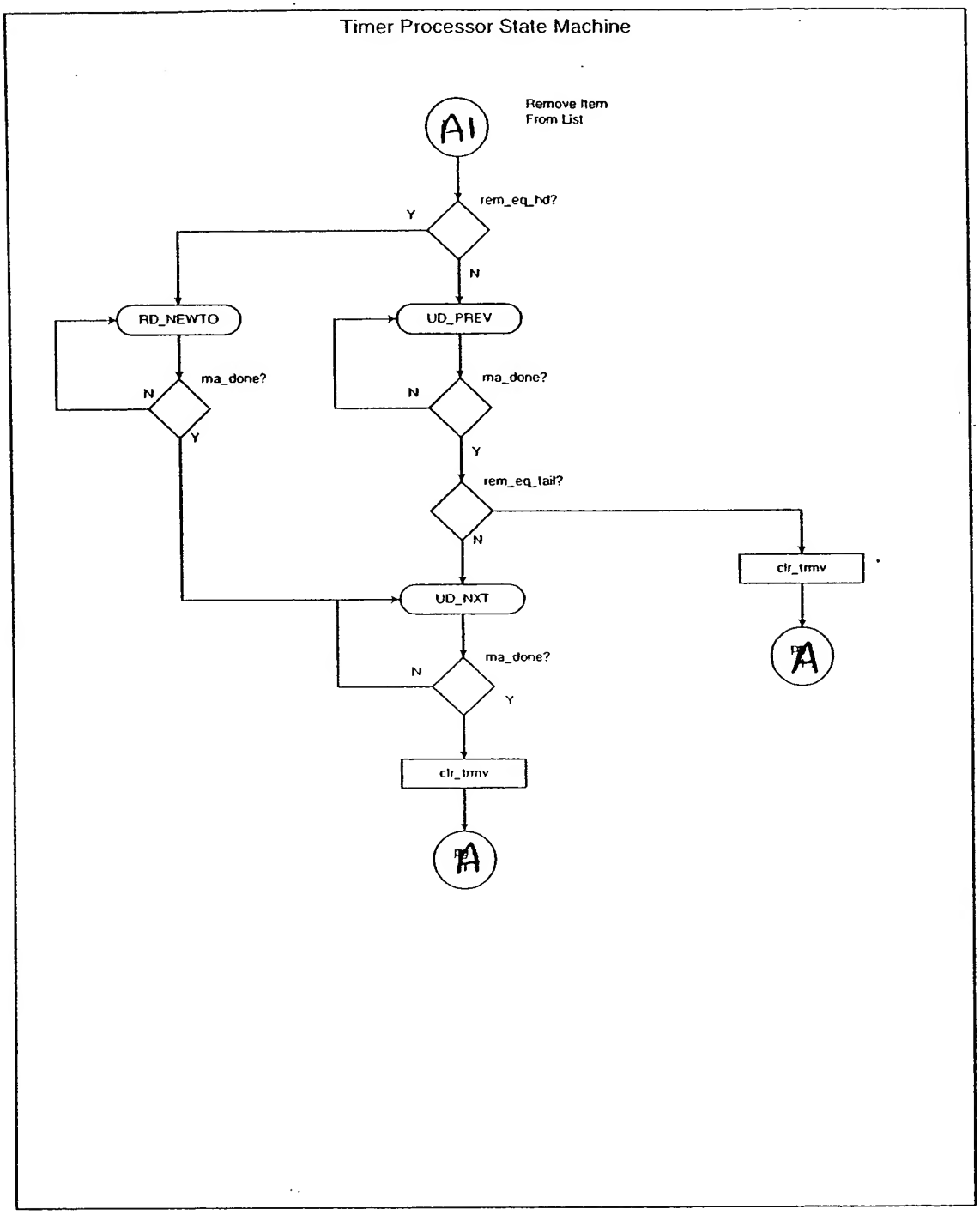

Timer Processor State Machine
A1
Remove Item
From List
rem_eq_hd?
Y
N
RD_NEWTO
ma_done?
N
Y
UD_PREV
ma_done?
N
Y
rem_eq_tail?
N
clr_tmv
UD_NXT
ma_done?
N
Y
clr_tmv

Figure 3L9B:

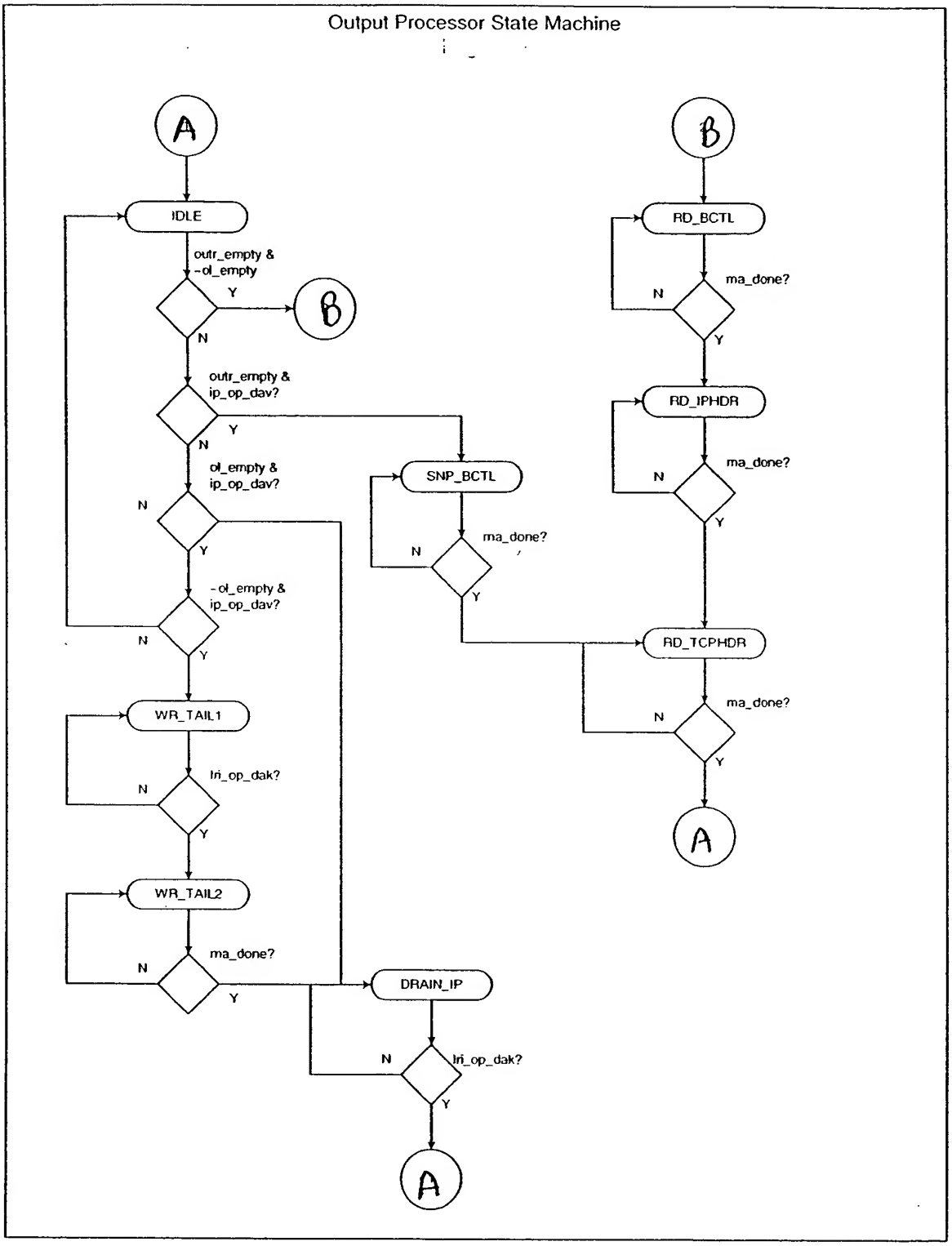

Output Processor State Machine
A
IDLE
outr_empty &
-ol_empty
Y
B
N
outr_empty &
ip_op_dav?
Y
N
ol_empty &
ip_op_dav?
N
Y
-ol_empty &
ip_op_dav?
N
Y
WR_TAIL1
lri_op_dak?
N
Y
WR_TAIL2
ma_done?
N
Y
DRAIN_IP
lri_op_dak?
N
Y
A
SNP_BCTL
ma_done?
N
Y
B
RD_BCTL
ma_done?
N
Y
RD_IPHDR
ma_done?
N
Y
RD_TCPHDR
ma_done?
N
Y
A

Figure 3L10 -

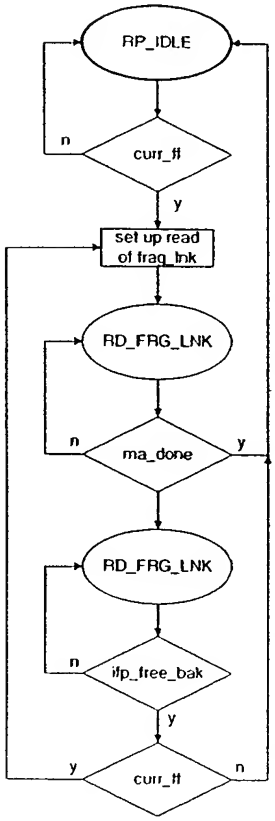


Figure 3L11 - Return Processor State Machine

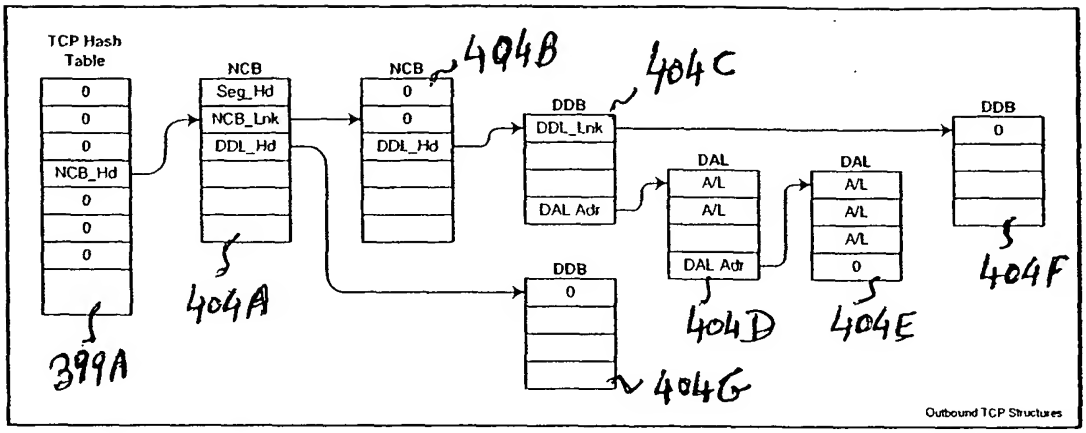


Figure 4A

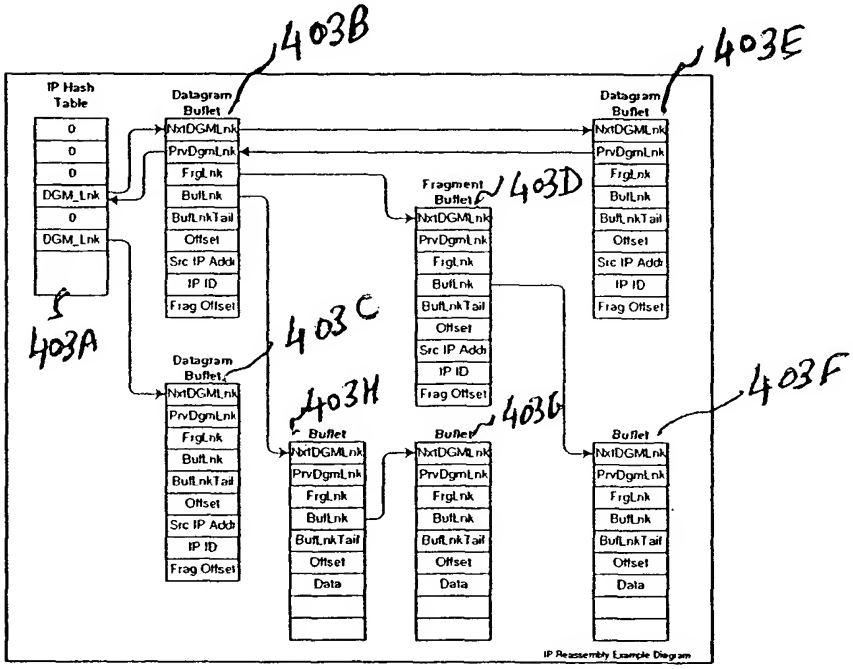


Figure 4B

403